Nexar / Protel 2004 Interface for the XSA-100 Board

Nexar is a multi-vendor, feature-rich FPGA design environment within a single IDE. It provides many industry standard soft processor cores complete with integrated build and debugging tools and virtual instruments such as logic analysers, frequency counters, frequency generators and I/O modules.

While the CPLDs and FPGAs are programmed by a standard hardware JTAG interface, the soft core debuggers and virtual instruments communicate via a second soft JTAG link based around the Nexus 5001 specification.

The XSA-100 Spartan 2 development board from XESS Corp. has a XC9572XL CPLD that acts as the interface between the Parallel Port and the Spartan II FPGA. XESS has published an application note and example code to emulate the Xilinx Parallel Cable III interface enabling the XSA-100 board to be seamlessly programmed from Xilinx's Impact programming tool.

This interface builds upon the XESS application note by adding Nexar Soft JTAG chain functionality to the XESS XSA-100 board enabling it to be used with Nexar, while still remaining backwards compatible with the Parallel Cable III and the Impact software.

Setting up your XESS XSA Board

1. Place JP9 in the XS (Xess) position on the XSA Board.
2. Power up the board and open the XESS GXSLoad utility.
3. Download the nexar_if.svf file into the CPLD by dragging the file onto the FPGA/CPLD list box and clicking on load.
4. Once downloaded, power down the board and place JP9 into the XI (Xilinx) position.

Setting up your DXP2004 Software

Copy the XESSXSA.JTGBRD (JTAG Board File) to your DXP2004 System Directory (C:\program files\altium2004\system)

(Note : It appears DXP2004 will open .JTGBRD files in alphabetical order. Therefore DXP2004 should open the XESSXSA.JTGBRD board file before the simular Xilinx.JTGBRD. If not, the soft chain will not function correctly)

Assigning Soft JTAG pins in your designs

The nexar_if.svf assigns the following pins be used for the Soft JTAG interface :

```
Record=Constraint | TargetKind=Port | TargetId=NEXUS_TDI      | PinNum=P50
Record=Constraint | TargetKind=Port | TargetId=NEXUS_TDO      | PinNum=P78
Record=Constraint | TargetKind=Port | TargetId=NEXUS_TCK      | PinNum=P47
Record=Constraint | TargetKind=Port | TargetId=NEXUS_TMS      | PinNum=P48
```

Due to limited resources between the Interface CPLD and the Spartan II FPGA, TDI, TCK & TMS share some of the address lines of the on-board FLASH memory. VHDL Source for the nexar_if is included should you wish to relocate these pins to better suit your requirements.

Example / Test Project

A simple example of a counter utilising the XSA's 7 Segment display and including a frequency counter, frequency generator and general purpose I/O module is included.

References :

Altium AP0119 : Using DXP2004 with a 3rd Party Board.
XESS App Note : Parallel Cable III Emulator for the XSA Board.

Altium Nexar : http://www.altium.com/nexar
Xess XSA Board : http://www.xess.com/