		<u> </u>			Φ.	- σ				_			Į
s	2	<u>ج</u>	Push-buttons	1	VGA Interface	PS/2 Interface		Stereo Codec		<u></u>	_		
XS95 Pins (J2)	Power/ GND	DIP Switch	put	1	ntel	l te		၂ ပို	2	PC Parallel Port	Oscillator		
95	wer	လွ်	Sh-I	LEDs	¥.	2	RAMs		8051 Uc	ے ^{ہے} ا	l iji		
XS:	Po	占			9	PS	RA	Ste	806	<u> </u>	Ö	Function	
1				LSB0			A4					Left LED segment; RAM address line	
2		4		LSB1			Α7	4		4		Left LED segment: RAM address line	
3				LSB2			A5					Left LED segment; RAM address line Uncommitted XS95 I/O pin	
5		DIPSW4						SDOUT	P1.3			DIP switch; codec serial data output; uC I/O	
6	6	DIPSW1					LCEB		P1.0			DIP switch; left RAM chip-enable, uC I/O port	
7	7	DIPSW2					RCEB		P1.1			DIP switch; right RAM chip-enable, uC I/O port	
9			RESETB	<u> </u>				<u> </u>	VTAL1	<u></u>		XS Board oscillator	
10 11		DIPSW3	_	<u>\$</u>					XTAL1 P1.2	<u></u>		Pushbutton; uC clock DIP switch; codec master clock; uC I/O port	
12		Dii 0				_		IVICE	FILE			Uncommitted XS95 I/O pin	
13	3								PSENB			uC program store-enable	
14				S5	RED1							XS Board LED segment; VGA color signal	
15 17		4		S6	HSYNCE			4		<u></u>		XS Board LED segment; VGA color signal	
17 18				S3 S4	GREEN1 RED0							XS Board LED segment; VGA color signal XS Board LED segment; VGA color signal	
19		/ /		S2	GREENO	0						XS Board LED segment; VGA color signal	j
20)								ALEB			uC address-latch-enable	
21				S0	BLUE0							XS Board LED segment; VGA color signal	
23				S1	BLUE1							XS Board LED segment; VGA color signal	j
25 26		4				VP CIT		4	D2 4 (T	21		Uncommitted XS95 I/O pin PS/2 keyboard clock; uC I/O port	İ
26 28						KB_CLK			P3.4 (T0	<u>))</u>		PS/2 keyboard clock; uC I/O port JTAG TDI; DIN	İ
28		/ 7		_		_						JTAG TMS	j
30)	/ 		_				_				JTAG TMS JTAG TCK; CCLK	j
31									P3.0 (R)			uC I/O port	İ
32									P3.7 (RI	RD_)		uC I/O port	İ
33									P3.5 (T1	1)		uC I/O port	j
34 35		4		RDPB DB8		4	D7		P2.7 P0.7	4		Right LED decimal-point; RAM address line; uC I/O port LED; RAM data line; uC muxed address/data line	İ
36		4		DB7			D6		P0.7			LED; RAM data line; uC muxed address/data line LED; RAM data line; uC muxed address/data line	İ
37		/ /		DB6			D5	_	P0.5			LED; RAM data line; uC muxed address/data line	İ
39)			DB5			D4		P0.4			LED; RAM data line; uC muxed address/data line	
40)			DB4			D3		P0.3			LED; RAM data line; uC muxed address/data line	İ
41				DB3			D2		P0.2			LED; RAM data line; uC muxed address/data line	
43 44		4		DB2 DB1			D1 D0	4	P0.1 P0.0	4		LED; RAM data line; uC muxed address/data line LED; RAM data line; uC muxed address/data line	
44 45				DBI			Du		RST	<u></u>		LED; RAM data line; uC muxed address/data line uC reset	
45		/ / /						CCLK	KOI	PC_D0		Codec control line; PC parallel port data output	
47		/ /		_		_		CDIN		PC_D1		Codec control line; PC parallel port data output	
48	3							CSB		PC_D2		Codec control line; PC parallel port data output	
	GND									- 20		Power supply ground	
50		4		<u> </u>		4		4		PC_D3		PC parallel port data output	
51 52		4				4				PC_D4 PC_D5		PC parallel port data output PC parallel port data output	
53		4		RSB4			A12		P2.4	PO_DO_		Right LED segment; RAM address line; uC I/O port	
54		/ 7		RSB2			A10		P2.2			Right LED segment; RAM address line; uC I/O port	
55	5			RSB3			A11		P2.3			Right LED segment; RAM address line; uC I/O port	
56	6			RSB1			A9		P2.1			Right LED segment; RAM address line; uC I/O port	
57				RSB5			A13		P2.5			Right LED segment; RAM address line; uC I/O port	
58 59				RSB0		<u>'</u>	A8		P2.0			Right LED segment; RAM address line; uC I/O port JTAG TDO; DOUT	
61		/ /		RSB6		<u></u>	A14		P2.6			Right LED segment; RAM address line; uC I/O port	
62		/ 		KODO	_		OEB		Γ Ζ.0			RAM output-enable	
63	3						WEB	_	P3.6 (W	<mark>/R_) _</mark>		RAM write-enable; uC I/O port	
65	5						CEB		,			XS Board RAM chip-enable	
66		DIPSW7						LRCK		PC_S5		DIP switch; codec left-right channel select; uC I/O port; PC	Sparallel port status in
68		<u> </u>		<u> </u>					P3.3 (IN			uC I/O port	
69 70		DIPSW8				KB_DAT	τΛ		P3.2 (IN	XD(C_S6		uC I/O port DIP switch; PS/2 keyboard serial data; uC I/O port; PC part	rallal part etatus input
70		DIPSW8				ND_υ	A		P1.5	PC_S3		DIP switch; codec serial input data; uC I/O port; PC paralle	el nort status input
72	2	DIPSW5		_		_				PC_S4		DIP switch; codec serial clock; uC I/O port; PC parallel port	
74	ı e											Uncommitted XS95 I/O pin	
75				LSB3			A0					Left LED segment; RAM address line	
76		4				4'		4		4		Uncommitted XS95 I/O pin	
77 78	8 +5V	4		_		4						Uncommitted XS95 I/O pin +5V power source	
78		/ / /		LSB4			A1					Left LED segment; RAM address line	
80)	/ 					7	_		PC_D7		PC parallel port data output	
81										PC_D6		PC parallel port data output	
82				LSB5			A2					Left LED segment; RAM address line	
83		4		LSB6 LDPB			A6	4		4		Left LED segment; RAM address line	
24,67		4	SPAREB		VSYNCE		A3		P1.7			Left LED decimal-point; RAM address line Pushbutton; XS Board LED decimal-point; VGA horiz. sync	C I/O nort
24,01			SPANLL	שב	VOTINOL	· <u> </u>		4	P1.7			Pushbullon, AS Board LED decimal point, VOA nonz. gynt	C.; uC I/O port

