XS40 Pin	Connects to…	Description
25	S0, BLUE0	These pins drive the individual segments of the LED display (S0-S6 and DP). They also drive the color and horizontal sync signals for a VGA monitor.
26	S1, BLUE1	
24	S2, GREEN0	
20	S3, GREEN1	
23	S4, RED0	
18	S5, RED1	
19	S6, HSYNCB	
13	CLK	An input driven by the 12 MHz oscillator.
44	PC_D0	These pins are driven by the data output pins of the PC parallel port. Clocking signals can only be reliably applied through pins 44 and 45 since these have additional hysterisis circuitry. Pins 32 and 34 are mode signals for the FPGA so you must adjust your design to account for the way that the Foundation tools handle these pins.
45	PC_D1	
46	PC_D2	
47	PC_D3	
48	PC_D4	
49	PC_D5	
32	PC_D6	
34	PC_D7	
37	XTAL1	Pin that drives the uC clock input
36	RST	Pin that drives the uC reset input
29	ALEB	Pin that monitors the uC address latch enable
14	PSENB	Pin that monitors the uC program store enable
7	P1.0	These pins connect to the pins of Port 1 of the uC. Some of the pins are also connected to the status input pins of the PC parallel port. Pin 67 drives the vertical sync signal for a VGA monitor.
8	P1.1	
9	P1.2	
6	P1.3	
77	P1.4, PC_S4	
70	P1.5, PC_S3	
66	P1.6, PC_S5	
67	P1.7, VSYNCB	
69	P3.1(TXD), PC_S6	These pins connect to some of the pins of Port 3 of the uC. The uC has specialized functions for each of the port pins indicated in parentheses. Pin 62 connects to the data write pin of the uC and the write-enable pin of the RAM. Pin 69 connects to a status input pin of the PC parallel port.
68	P3.4(T0)	
62	P3.6(WRB), WEB	
27	P3.7(RDB)	
41	P0.0(AD0), D0	These pins connect to Port 0 of the uC which is also a multiplexed address/data port. These pins also connect to the data pins of the RAM.
40	P0.1(AD1), D1	
39	P0.2(AD2), D2	
38	P0.3(AD3), D3	
35	P0.4(AD4), D4	
81	P0.5(AD5), D5	
80	P0.6(AD6), D6	
10	P0.7(AD7), D7	
59	P2.0(A8), A8	These pins connect to Port 2 of the uC which also outputs the upper address byte. These pins also connect to the 7 upper address bits of the RAM.
57	P2.0(A9), A9	
51	P2.0(A10), A10	
56	P2.0(A11), A11	
50	P2.0(A12), A12	
58	P2.0(A13), A13	
60	P2.0(A14), A14	
28	P2.0(A15)	
3	A0	These pins drive the 8 lower address bits of the RAM.
4	A1	
5	A2	
78	A3	
79	A4	
82	A5	
83	A6	
84	A7	
61	OEB	Pin that drives the RAM output enable.
65	CEB	Pin that drives the RAM chip enable.
75	PC_S7	Pin that drives a status input pin of the PC parallel port.