A

XSA Pin Connections

The following tables list the pin numbers of the Spartan-II FPGA and the XC9572XL CPLD along with the pins of the other chips that they connect to on the XSA Board. The columns of the table are arranged as follows:

Column 1 lists the Spartan-II FPGA pin. It is left blank if there is no connection to the FPGA for this function. Pins marked with * are useable as general-purpose I/O through the prototyping header; pins marked with ** can be used as general-purpose I/O only if the CPLD interface is reprogrammed as described previously; pins with no marking cannot be used as general-purpose I/O at all.

Column 2 lists the XC9572XL CPLD pin. It is left blank if there is no connection to the CPLD for this function.

Column 3 lists the pins of other devices on the XSA Board that are connected to the associated FPGA and/or CPLD pin.

Column 4 lists the pin of the XSA prototyping header that is connected to the associated FPGA and/or CPLD pin.

Columns 5–7 list the pins of devices on the Xstend Board that will connect to the FPGA and/or CPLD when the XSA Board is inserted into an Xstend Board.

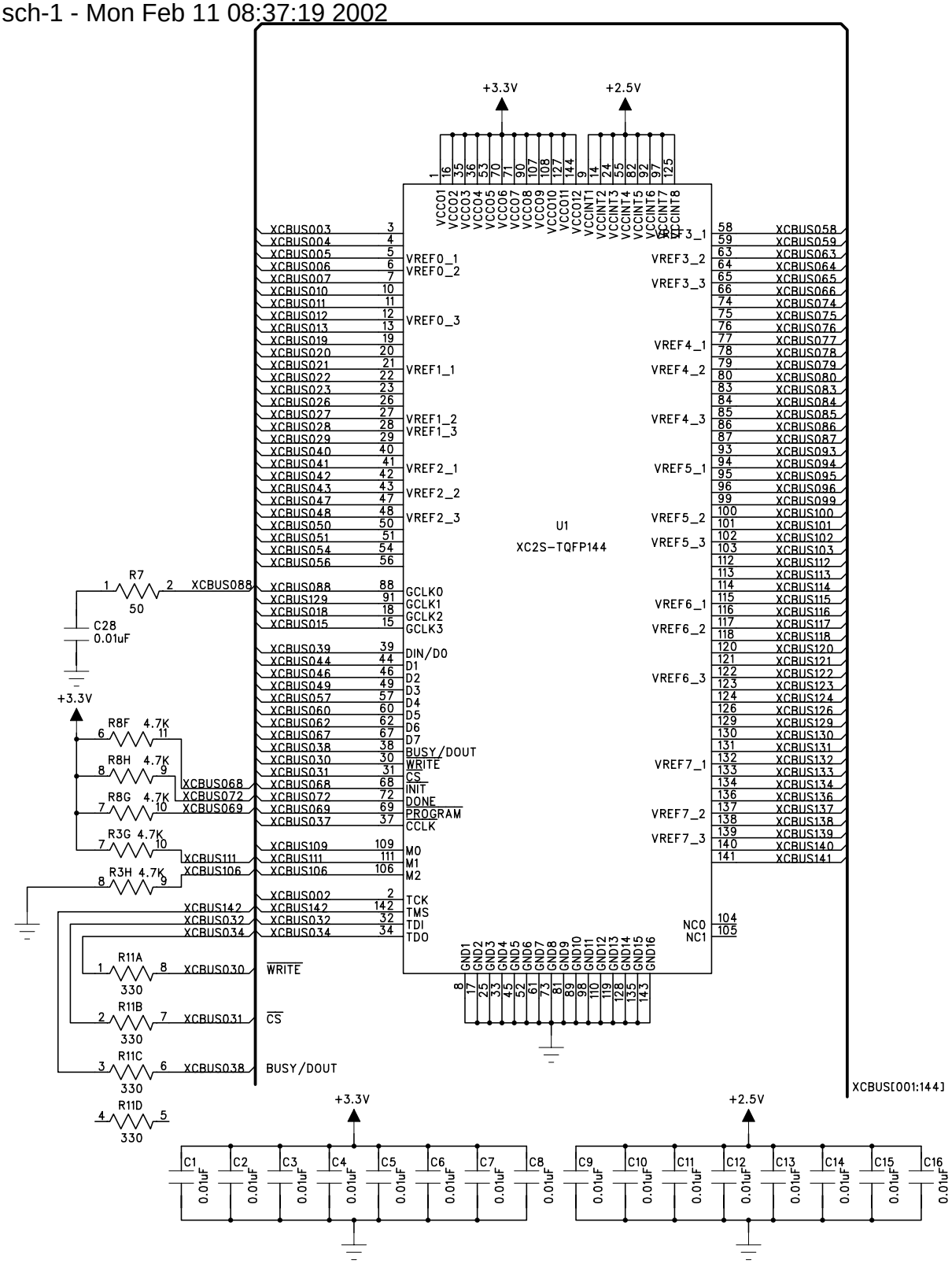
FPGA	CPLD	XSA Function	Proto. Pin	XSTend Functions		
1		+3.3V	54	+3.3V		
2	13	SPARTAN-TCK	16			Xchecker-TCK
3		SDRAM-A7				
4		SDRAM-A1				
5		SDRAM-A6				
6		SDRAM-A2				
7		SDRAM-A5				
8		GND	52	GND		
9		+2.5V	22			
10		SDRAM-A3				
11		SDRAM-A4				
12*		VGA-RED0	27			
13*		VGA-RED1	28	RAM-A15	RLED-/DP	
15*		SPARTAN-GCK3	31			
18*		SPARTAN-GCK2	1			
19*		VGA-GREEN0	29			
20*		VGA-GREEN1	32			Xchecker-RT
21*		VGA-BLUE0	33			
22*		VGA-BLUE1	34			
23*		VGA-/HSYNC	36			
26*		VGA-/VSYNC	37		Pushbutton-/RESET	
27*	62	FLASH-A3	50	RAM-A12	RLED-/S4	
28*	63	FLASH-A2, *PARPORT-S5	51	RAM-A10	RLED-/S2	
29*	64	FLASH-A1, *PARPORT-S4	56	RAM-A11	RLED-/S3	
30*	19	SPARTAN-/WRITE	69	PS2/DATA	DIPSW8	
31*	15	SPARTAN-CS	68	PS2/CLK		
32	15*	SPARTAN-TDI	15			Xchecker-TDI
34	19*	SPARTAN-TDO	30			Xchecker-RD
37	16	SPARTAN-CCLK	73			Xchecker-CCLK
38*	18	SPARTAN-DOUT/BSY	45			
39*	2	FLASH-D0,DIN/D0,LED-S1	71			Xchecker-DIN
40*	1	FLASH-A0, *PARPORT-S3	57	RAM-A9	RLED-/S1	
41*	11	FLASH-/CE	65	RAM-/CE		
42**	57	FLASH-A10, *PARPORT-D2	58	RAM-A13	RLED-/S5	
43**	12	FLASH-/OE, *PARPORT-D7	61	RAM-/OE		
44*	4	FLASH-D1,LED-DP	40	RAM-D1	BARLED-2	
46*	5	FLASH-D2,LED-S4	39	RAM-D2	BARLED-3	
47**	43	FLASH-A11, *PARPORT-D3	59	RAM-A8	RLED-/S0	
48**	44	FLASH-A9, *PARPORT-D1	60	RAM-A14	RLED-/S6	
49*	6	FLASH-D3,LED-S6	38	RAM-D3	BARLED-4	
50**	45	FLASH-A8, *PARPORT-D0	78	RAM-A3	LLED-/S3	
51**	46	FLASH-A13, *PARPORT-D5	79	RAM-A4	LLED-/S4	
54*	47	FLASH-A14,DIPSW1A	82	RAM-A5	LLED-/S5	
56*	48	FLASH-A17,DIPSW1D	83	RAM-A6	LLED-/S6	
57*	7	FLASH-D4,LED-S5	35	RAM-D4	BARLED-5	
58**	49	FLASH-/WE, *PARPORT-D6	62	RAM-WE		
59*	50	FLASH-/RESET	66	CODEC-LRCK	DIPSW7	
60*	8	FLASH-D5,LED-S3	80	RAM-D6	BARLED-7	
62*	9	FLASH-D6,LED-S2	81	RAM-D5	BARLED-6	
63*	51	FLASH-A16,DIPSW1C	84	RAM-A7	LLED-/DP	
64*	52	FLASH-A15,DIPSW1B	3	RAM-A0	LLED-/S0	
65**	56	FLASH-A12, *PARPORT-D4	4	RAM-A1	LLED-/S1	
66*	58	FLASH-A7	5	RAM-A2	LLED-/S2	
67*	10	FLASH-D7,LED-S0	10	RAM-D7	BARLED-8	
68*	38	SPARTAN-/INIT	41	RAM-D0	BARLED-1	Xchecker-INIT
69	39	SPARTAN-/PROGRAM	55		Pushbutton-/PROGRAM	Xchecker-PROG
72	40	SPARTAN-DONE	53			Xchecker-DONE
74*	61	FLASH-A4	70	CODEC-SDIN	DIPSW6	
75*	60	FLASH-A5	77	CODEC-SCLK	DIPSW5	
76*	59	FLASH-A6	6	CODEC-SDOUT	DIPSW4	
77*			9	CODEC-MCLK	DIPSW3	Xchecker-CLKO
78*		PARPORT-S6	67	VGA-/VSYNC	Pushbutton-/SPARE	
79*			7	RAM-/LCE	DIPSW1	Xchecker-TRIG

FPGA	CPLD	XSA Function	Proto. Pin	XSTend Functions		
80*			8	RAM-/RCE	DIPSW2	Xchecker-RST
83*			18	VGA-RED1		
84*			19	VGA-/HSYNC		
85*			20	VGA-GREEN1		
86*			23	VGA-RED0		
87*			24	VGA-GREEN0		
88	42	MASTER_CLK	13	MASTER_CLK		Xchecker-CLKI
91		SDRAM-CLK				
93*		PS2-DATA,PUSHBUTTON	25	VGA-BLUE0		
94*		PS2-CLK	26	VGA-BLUE1		
95		SDRAM-Q0				
96		SDRAM-Q15				
99		SDRAM-Q1				
100		SDRAM-Q14				
101		SDRAM-Q2				
102		SDRAM-Q13				
103		SDRAM-Q3				
106		SPARTAN-M2	12			
109	36	SPARTAN-M0	14			
111		SPARTAN-M1	21			
112		SDRAM-Q12				
113		SDRAM-Q4				
114		SDRAM-Q11				
115		SDRAM-Q5				
116		SDRAM-Q10				
117		SDRAM-Q6				
118		SDRAM-Q9				
120		SDRAM-Q7				
121		SDRAM-Q8				
122		SDRAM-QML				
123		SDRAM-/WE				
124		SDRAM-QMH				
126		SDRAM-/CAS				
129		SDRAM-CLK				
130		SDRAM-/RAS				
131		SDRAM-CKE				
132		SDRAM-/CS				
133		SDRAM-A12				
134		SDRAM-BA0				
136		SDRAM-A11				
137		SDRAM-BA1				
138		SDRAM-A9				
139		SDRAM-A10				
140		SDRAM-A8				
141		SDRAM-A0				
142	18*	SPARTAN-TMS	17			Xchecker-TMS
	30	PARPORT-C1,CPLD-TCK				
	29	PARPORT-C2,CPLD-TMS				
	28	PARPORT-C3,CPLD-TDI				
	33	PARPORT-D0				
	32	PARPORT-D1				
	31	PARPORT-D2				
	27	PARPORT-D3				
	25	PARPORT-D4				
	24	PARPORT-D5				
	23	PARPORT-D6				
	22	PARPORT-D7				
	34	PARPORT-S3				
	20	PARPORT-S4				
	35	PARPORT-S5				
	53	PARPORT-S7,CPLD-TDO				
	17	PROG-OSC				
			64	Osc-In		

B

XSA Schematics

The following pages show the detailed schematics for the XSA Board.



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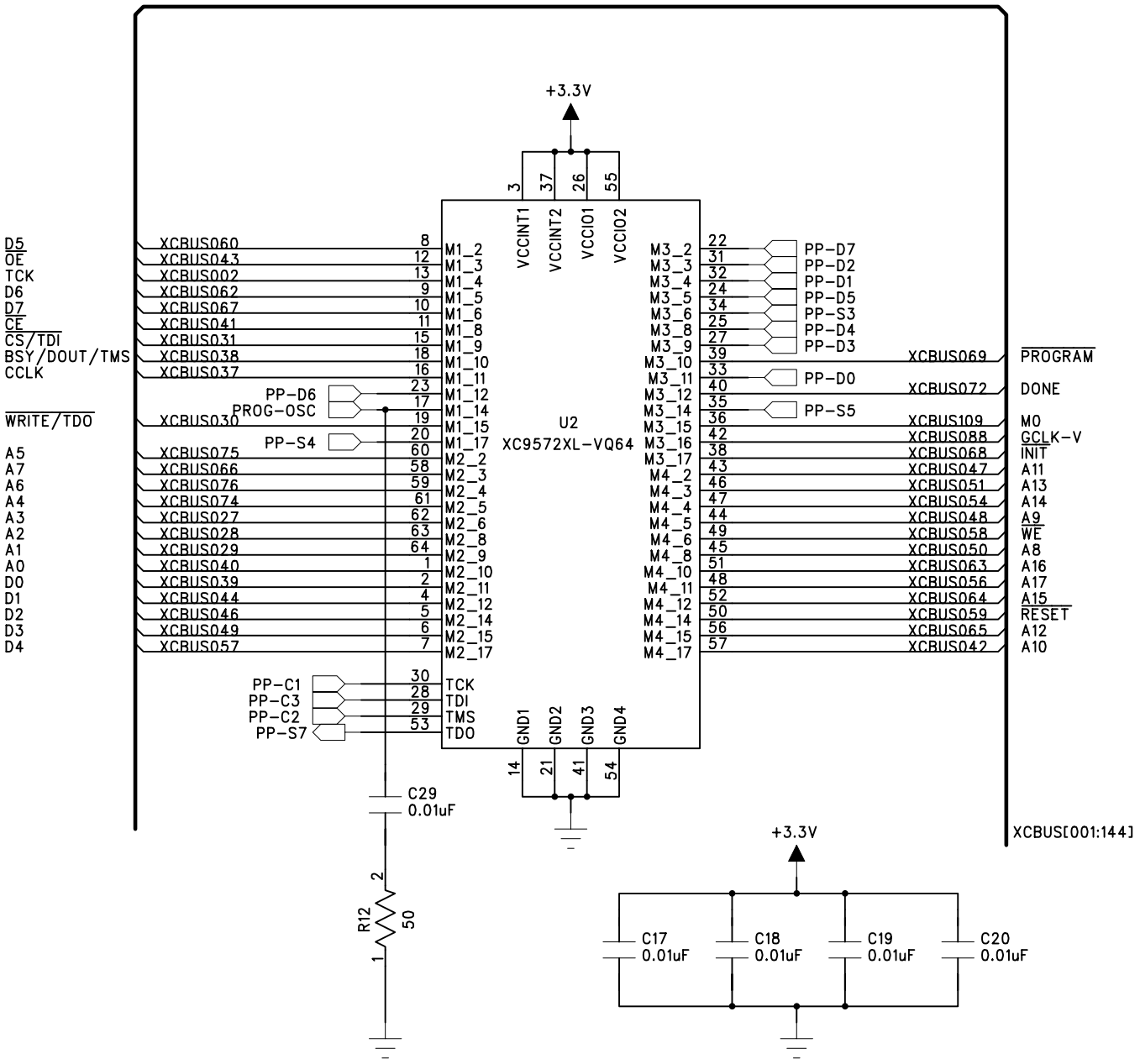
RELEASED:	DATED:	SHEET: OF



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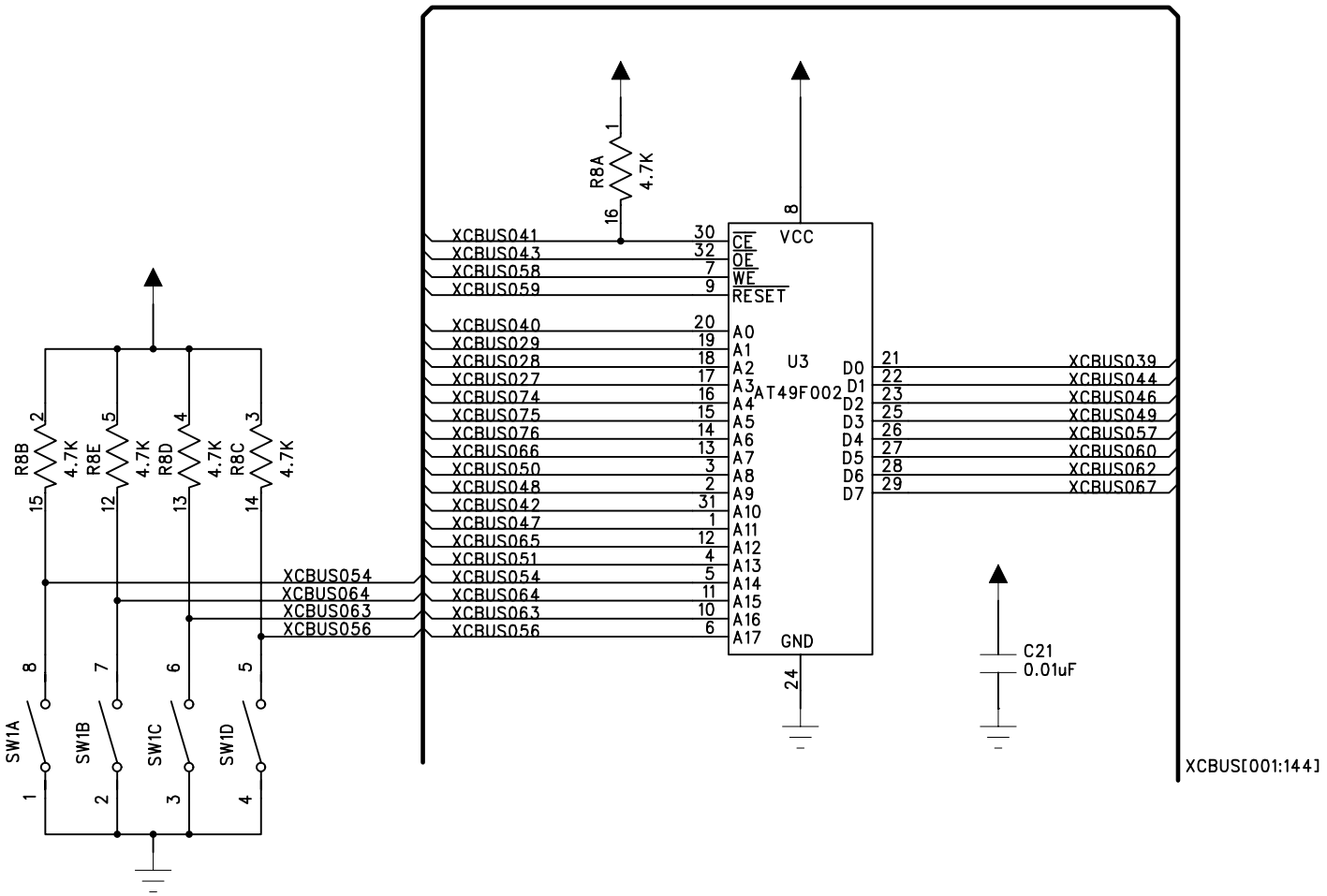
RELEASED:	DATED:	SHEET: OF



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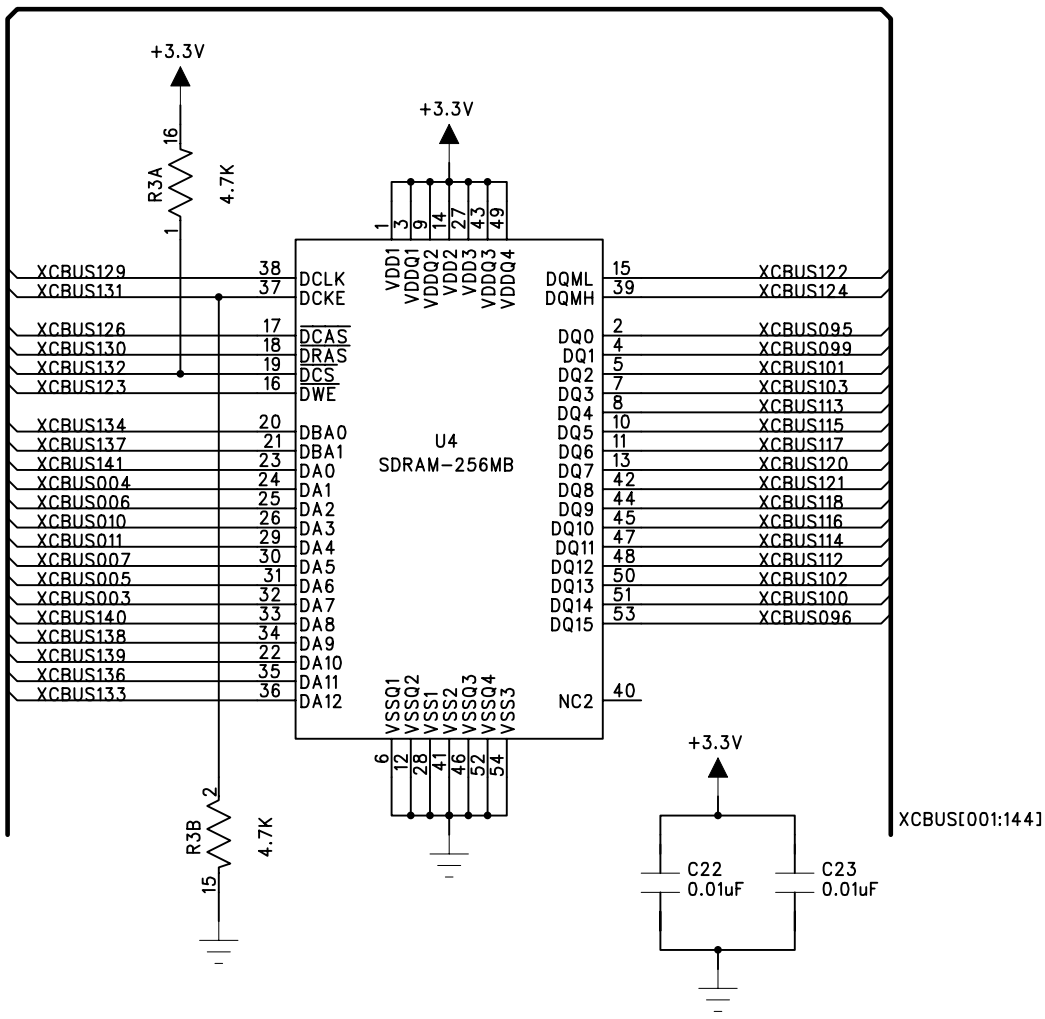
RELEASED:	DATED:	SHEET: OF



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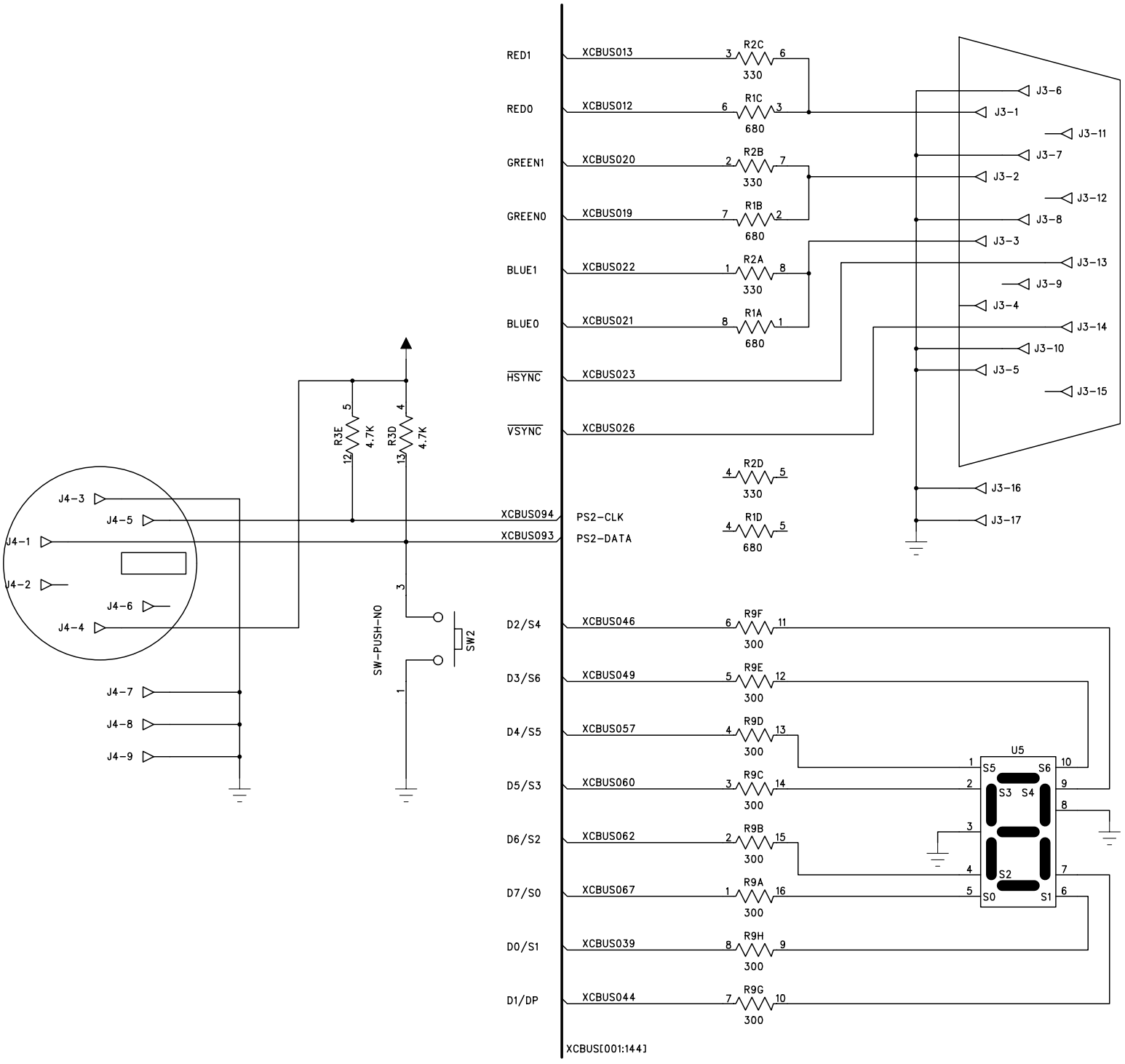

COMPANY: XESS Corporation		
TITLE: XSA Board PS/2 Port, VGA Port, LED		
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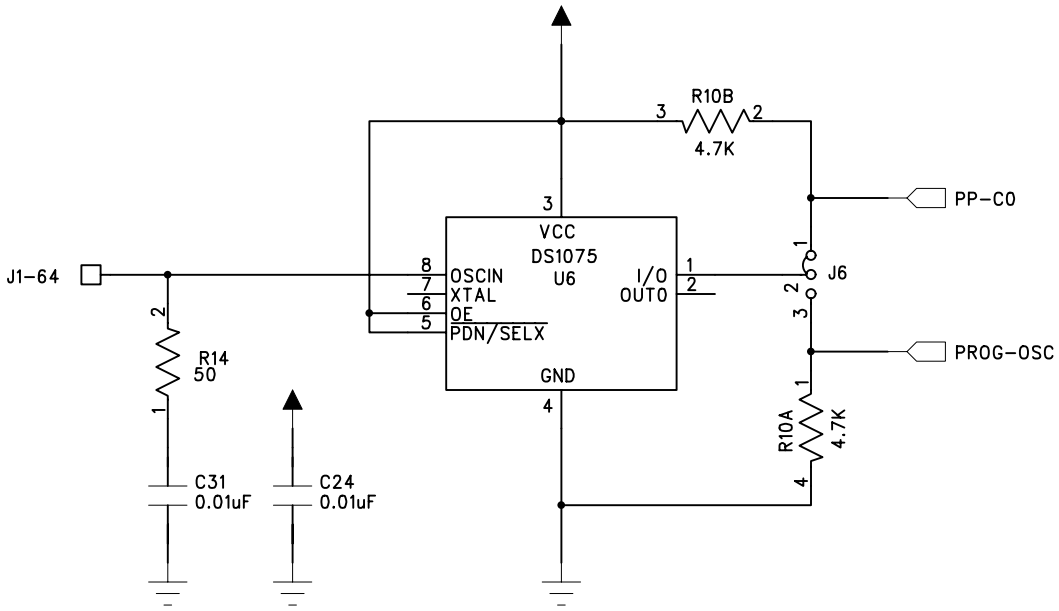
RELEASED:	DATED:	SHEET: OF



COMPANY: XESS Corporation		
TITLE: XSA Board Programmable Oscillator		
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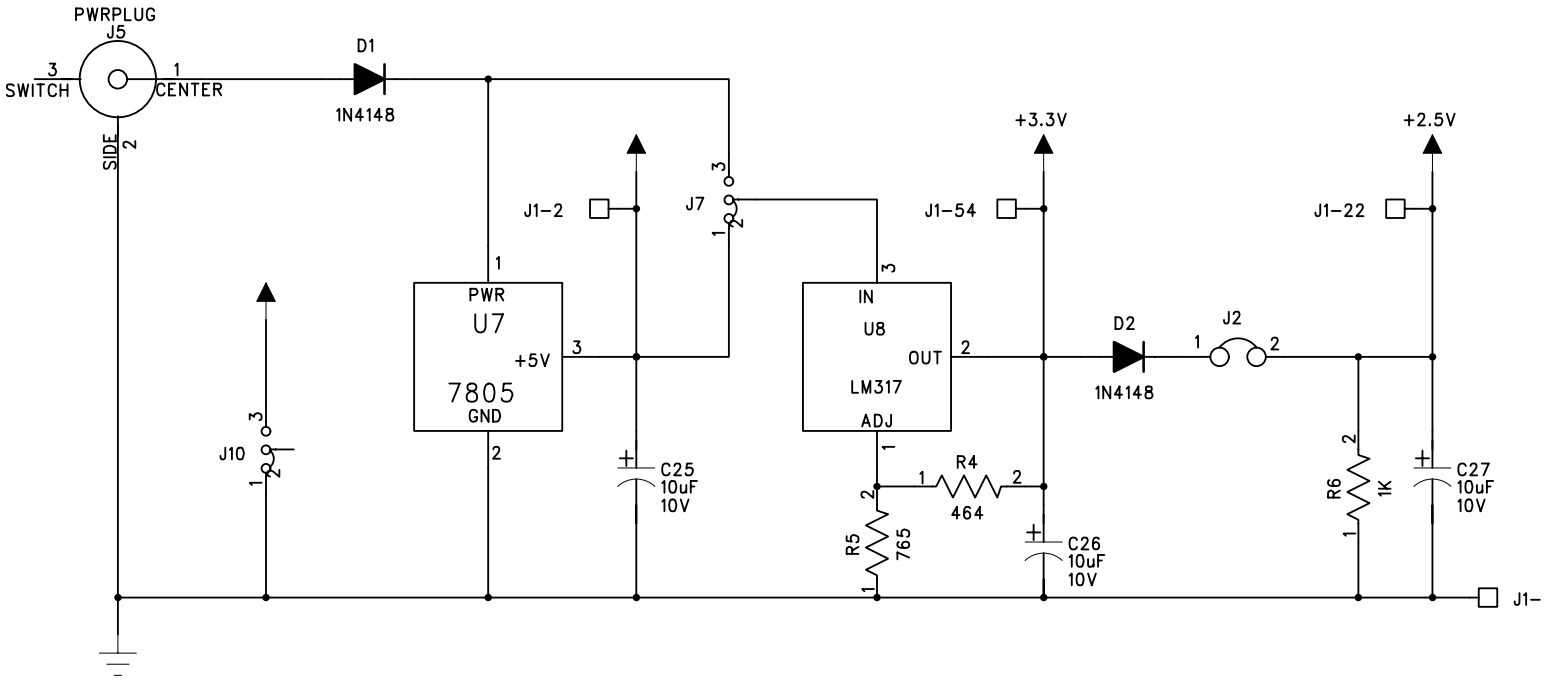
RELEASED:	DATED:	SHEET: OF



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TITLE: XSA Board Regulated Power Supplies		
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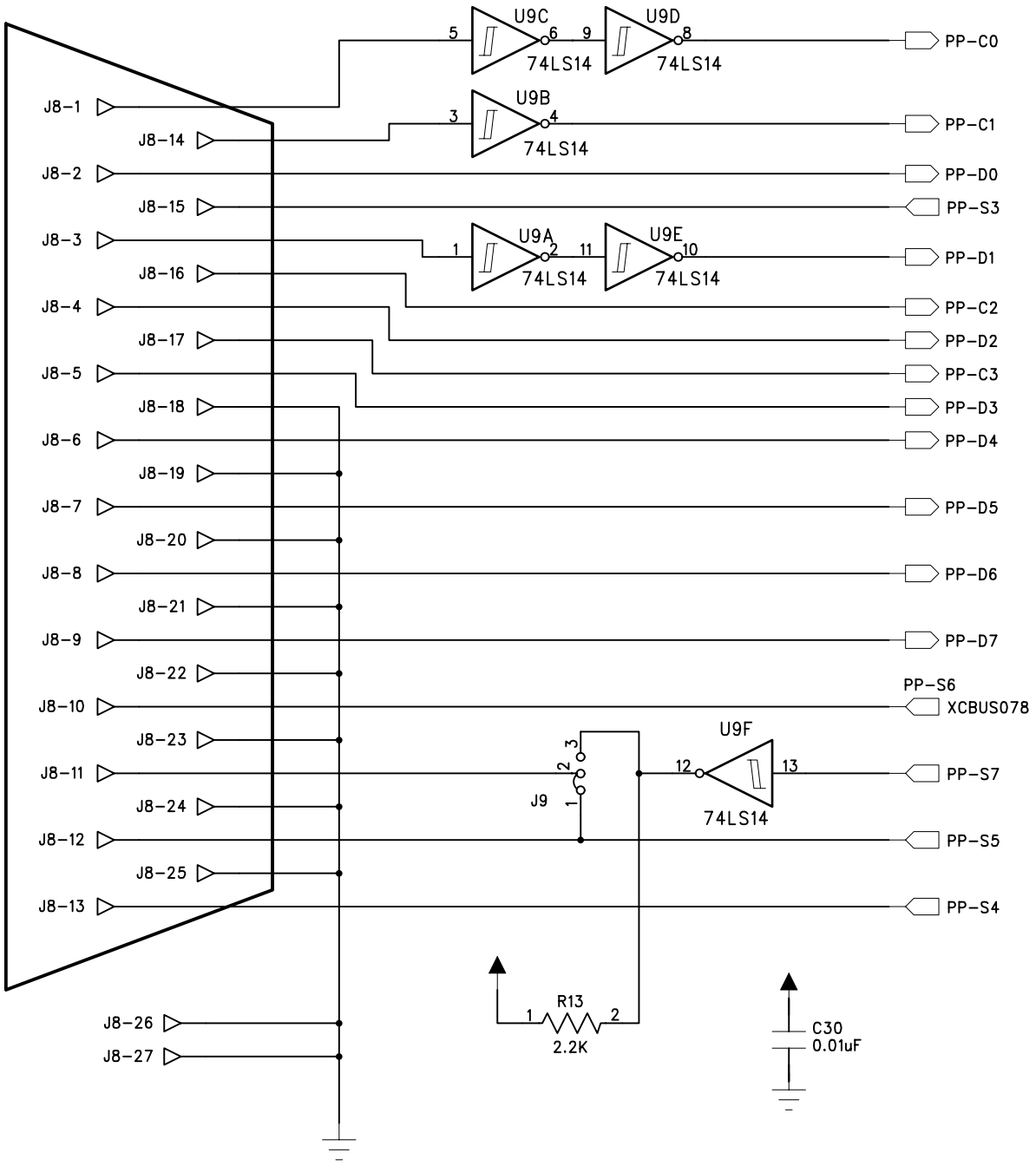
RELEASED:	DATED:	SHEET: OF



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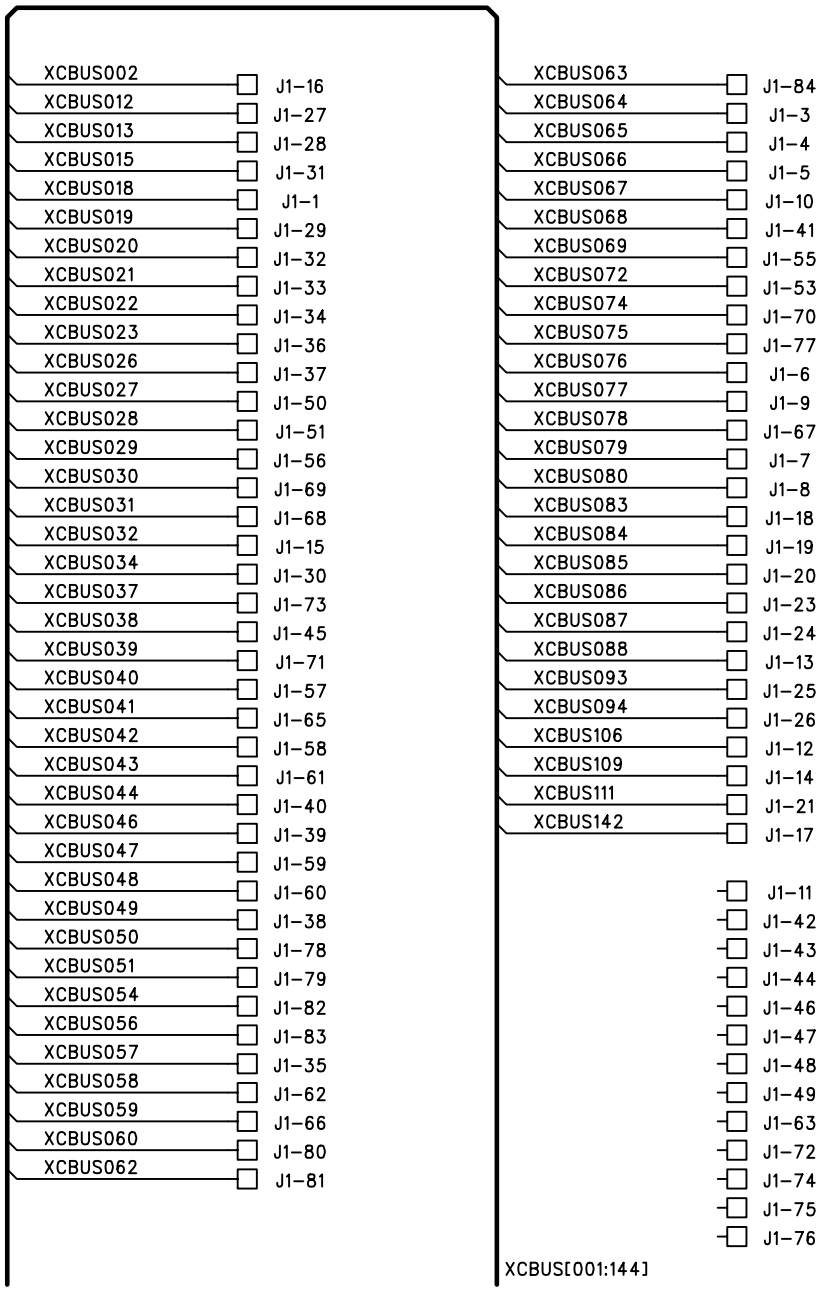
RELEASED:	DATED:	SHEET: OF



COMPANY: XESS Corporation		
TITLE: XSA Board Prototyping Header		
DRAWN:	DATED:	REV: V1.2
RELEASED:	DATED:	SHEET: OF

A

XSB Pin Connections

The following tables list the pin numbers of the FPGA and CPLD along with the pin names of the other chips that they connect to. These connections correspond with the pin assignments in the user-constraint files FPGA.UCF and CPLD.UCF.

Connections Between the FPGA and Other XSB Board Components

FPGA Pin	FPGA Pin Function	Net Name	CPLD	Flash	SRAM	SDRAM	Video Dcdr.	ADC	Video DAC	Stereo Codec	Ether-net	USB	Serial Port	IDE Intfc.	Cmpct. Flash	Switch Button	LEDs	JP5	JP7	Prog. Osc.
1	GND																			
2	TMS	FPGA-BSY/DOUT/TMS	18																	
3		ADC-CLK						CLK												
4		ADC-OE#						OE#												
5		I2C-SDA					SDA													SDAT
6		I2C-SCL					SCL													SCLK
7		VIDOUT-VSYNC#																3		
8		VIDOUT-HSYNC#																4		
9		VIDOUT-GY0							GY0									5		
10		VIDOUT-GY1							GY1									6		
11		VIDOUT-GY2							GY2									7		
12	GND																			
13	VCCO																			
14	VCCINT																			
15		VIDOUT-GY3							GY3									8		
16		VIDOUT-GY4							GY4									9		
17		VIDOUT-GY5							GY5									10		
18		VIDOUT-GY6							GY6									11		
19	GND																			
20		VIDOUT-GY7							GY7									12		
21		VIDOUT-GY8							GY8									13		
22		VIDOUT-GY9							GY9									14		
23		VIDOUT-CLK							CLK									15		
24		VIDOUT-BLANK#							BLANK#									16		
25	GND																			
26	VCCO																			
27		VIDOUT-RCR9							RCR9									17		
28	VCCINT																			
29		VIDOUT-RCR8							RCR8									18		
30		VIDOUT-RCR7							RCR7									19		
31		VIDOUT-RCR6							RCR6									20		
32	GND																			
33		VIDOUT-RCR5							RCR5									21		
34		VIDOUT-RCR4							RCR4									22		
35		VIDOUT-RCR3							RCR3									23		
36		VIDOUT-RCR2							RCR2									24		
37	VCCINT																			
38	VCCO																			
39	GND																			
40		VIDOUT-RCR1							RCR1									25		
41		VIDOUT-RCR0							RCR0									26		
42		VIDOUT-BCB0							BCB0									27		
43		VIDOUT-BCB1							BCB1									28		
44		VIDOUT-BCB2							BCB2									29		
45		VIDOUT-BCB3							BCB3									30		
46		VIDOUT-BCB4							BCB4									31		
47		VIDOUT-BCB5							BCB5									32		
48		VIDOUT-BCB6							BCB6									33		
49		VIDOUT-BCB7							BCB7									34		
50	M1	FPGA-M1(+3.3V)																		
51	GND																			
52	M0	FPGA-M0	36																	
53	VCCO																			
54	M2	FPGA-M2(GND)																		
55		VIDOUT-BCB8																35		
56		VIDOUT-BCB9																36		
57		FLASH-CE#	11	CE#																
58		PB-ECS0#																	43	
59		NV-CS0#												CS0#	CE1#/CE1#/CS0#					
60		NV-CS1#												CS1#	CE2#/CE2#/CS1#					
61		NV-INTRQ												INTRQ	RDY-BSY/IREQ/INTRQ					
62		NV-IORDY												IORDY	WAIT#/WAIT#/IORDY					
63		NV-IOCS16												IOCS16#	WP/IOIS16#/IOCS16#					
64		NV-DMACK#												DMACK#						
65	GND																			
66	VCCO																			
67	VCCINT																			
68		NV-DMARQ												DMARQ						
69		RS232-CTS														CTS				
70		RS232-RTS														RTS				
71		RS232-TD														TD				

Connections Between the FPGA and Other XSB Board Components

FPGA Pin	FPGA Pin Function	Net Name	CPLD	Flash	SRAM	SDRAM	Video Dcdr.	ADC	Video DAC	Stereo Codec	Ether-net	USB	Serial Port	IDE Intfc.	Cmpct. Flash	Switch Button	LEDs	JP5	JP7	Prog. Osc.
72	GND																			
73		RS232-RD														RD				
74		ETHERNET-IOCS16#									IOCS16#									
75		ETHERNET-IREQ									IREQ									
76	VCCINT																			
77	I/GCK1	FPGA-CLK1																		CLKD
78	VCCO																			
79	GND																			
80	I/GCK0	SDRAM-CLK																		CLKB
81		ETHERNET-RDY/DTACK									RDY/DTACK									
82		ETHERNET-CS#									CS#									
83		PB-A0	1	A0	A0	A0					SA0	FIFOADR0		DA0	A00		BAR1		23	
84		PB-A1	64	A1	A1	A1					SA1	FIFOADR1		DA1	A01		BAR2		24	
85	GND																			
86		PB-A2	63	A2	A2	A2					SA2	FIFOADR2		DA2	A02		BAR3		25	
87		PB-A3	62	A3	A3	A3					SA3				A03		BAR4		26	
88		PB-A4	61	A4	A4	A4					SA4				A04		BAR5		27	
89		PB-A5	60	A5	A5	A5					SA5				A05		BAR6		28	
90	VCCINT																			
91	VCCO																			
92	GND																			
93		PB-A6	59	A6	A6	A6					SA6				A06		BAR7		29	
94		PB-A7	58	A7	A7	A7					SA7				A07		BAR8		30	
95		SDRAM-WE#				WE#														
96		SDRAM-CAS#				CAS#														
97		SDRAM-RAS#				RAS#														
98		SDRAM-CE#				CE#														
99		SDRAM-CKE				CKE														
100		PB-A8	45	A8	A8	A8					SA8				A08	S1			31	
101		PB-A9	44	A9	A9	A9					SA9				A09	S2			32	
102		PB-A10	57	A10	A10	A10									A10	S3			33	
103	GND																			
104	DONE	FPGA-DONE	40																	
105	VCCO																			
106	PROGRAM#	FPGA-PROGRAM#	39													S7				
107	INIT#	FPGA-INIT#	38																	
108	D7	PB-D7	10	D7	D7	D7					D7	FD7		DD7	D07		LEFT-DP		14	
109		PB-A11	43	A11	A11	A11										S4			34	
110		PB-A12	56	A12	A12	A12										S5-1			35	
111		PB-A13	46	A13	A13	BA0										S5-2			36	
112		PB-A14	47	A14	A14	BA1										S5-3			37	
113		PB-A15	52	A15	A15											S5-4			38	
114		PB-A16	51	A16	A16											S5-5			39	
115		PB-A17	48	A17	A17							PKTEND			REG#	S5-6			40	
116	D6	PB-D6	9	D6	D6	D6					D6	FD6		DD6	D06		LEFT-G		13	
117	GND																			
118	VCCO																			
119	VCCINT																			
120	D5	PB-D5	8	D5	D5	D5					D5	FD5		DD5	D05		LEFT-F		12	
121		PB-A18	42	A18								SLRD		DIOR#	IORD#	S5-7			41	
122		PB-A19	50									SLWR		DIOW#	IOWR#	S5-8			42	
123		PB-WE#	49	WE#	WE#	WE#					IOWR#				WE#				4	
124	GND																			
125		PB-OE#	12	OE#	OE#	OE#					IORD#	SLOE			OE#/OE#/ATA_SEL#				3	
126	D4	PB-D4	7	D4	D4	D4					D4	FD4		DD4	D04		LEFT-E		11	
127		PB-D8			D8	D8					D8	FD8		DD8	D08		RIGHT-A		15	
128	VCCINT																			
129		PB-D9			D9	D9					D9	FD9		DD9	D09		RIGHT-B		16	
130	VCCO																			
131	GND																			
132		PB-D10			D10	D10					D10	FD10		DD10	D10		RIGHT-C		17	
133		PB-D11			D11	D11					D11	FD11		DD11	D11		RIGHT-D		18	
134		PB-D12			D12	D12					D12	FD12		DD12	D12		RIGHT-E		19	
135	D3	PB-D3	6	D3	D3	D3					D3	FD3		DD3	D03		LEFT-D		10	
136		PB-D13			D13	D13					D13	FD13		DD13	D13		RIGHT-F		20	
137	GND																			
138		PB-D14			D14	D14					D14	FD14		DD14	D14		RIGHT-G		21	
139		PB-D15			D15	D15					D15	FD15		DD15	D15		RIGHT-DP		22	
140		PB-LB#			LB#	LDQM					AEN/PSEN						BAR9		5	
141	D2	PB-D2	5	D2	D2	D2				CDTO	D2	FD2		DD2	D02		LEFT-C		9	
142	VCCINT																			

Connections Between the FPGA and Other XSB Board Components																				
FPGA Pin	FPGA Pin Function	Net Name	CPLD	Flash	SRAM	SDRAM	Video Dcdr.	ADC	Video DAC	Stereo Codec	Ether-net	USB	Serial Port	IDE Intfc.	Cmpct. Flash	Switch Button	LEDs	JP5	JP7	Prog. Osc.
143	VCCO																			
144	GND																			
145	D1	PB-D1	4	D1	D1	D1				CDTI	D1	FD1		DD1	D01		LEFT-B		8	
146		PB-UB#			UB#	UDQM					BHE#						BAR10		6	
147		RAM-CE#			CE#	CE#														
148		USB-CS#										CS#								
149		USB-INT#										INT#								
150		USB-READY										READY								
151		USB-FLAGC										FLAGC								
152		USB-FLAGB										FLAGB								
153	DIN/D0	PB-D0	2	D0	D0	D0				CCLK	D0	FD0		DD0	D00		LEFT-A		7	
154	DOUT/BUSY	FPGA-BSY/DOUT/TMS	18																	
155	CCLK	FPGA-CCLK	16																	
156	VCCO																			
157	TDO	FPGA-WRITE#/TDO	19																	
158	GND																			
159	TDI	FPGA-CS#/TDI	15																	
160	CS#	FPGA-CS#/TDI	15																	
161	WRITE#	FPGA-WRITE#/TDO	19																	
162		USB-FLAGA										FLAGA								
163		USB-IFCLK										IFCLK								
164		USB-VBUS																		
165		AU-CSN#								CSN#										
166		AU-BCLK								BCLK										
167		AU-MCLK								MCLK										
168		AU-LRCK								LRCK										
169		AU-SDTI								SDTI										
170	GND																			
171	VCCO																			
172	VCCINT																			
173		AU-SDTO0								SDTO0										
174		VIDIN-HPD0					HPD0	D8												
175		VIDIN-HPD1					HPD1	D9												
176		VIDIN-HPD2					HPD2	D10												
177	GND																			
178		VIDIN-HPD3					HPD3	D11												
179		VIDIN-HPD4					HPD4	OVRNG												
180		VIDIN-HPD5					HPD5												44	
181		VIDIN-HPD6					HPD6												45	
182	I/GCK2	FPGA-CLK0																		CLKC
183	GND																			
184	VCCO																			
185	I/GCK3	VIDIN-ICLK					ICLK													
186	VCCINT																			
187		VIDIN-HPD7					HPD7												46	
188		VIDIN-IPD0					IPD0	D0												
189		VIDIN-IPD1					IPD1	D1												
190	GND																			
191		VIDIN-IPD2					IPD2	D2												
192		VIDIN-IPD3					IPD3	D3												
193		VIDIN-IPD4					IPD4	D4												
194		VIDIN-IPD5					IPD5	D5												
195	VCCINT																			
196	VCCO																			
197	GND																			
198		VIDIN-IPD6					IPD6	D6												
199		VIDIN-IPD7					IPD7	D7												
200		VIDIN-IGPH					IGPH													
201		VIDIN-IGPV					IGPV													
202		VIDIN-IGP1					IGP1													
203		VIDIN-IGP0					IGP0													
204		VIDIN-ITRI					ITRI													
205		VIDIN-IDQ					IDQ													
206		VIDIN-ITRDY					ITRDY													
207	TCK	FPGA-TCK	13																	
208	VCCO																			

Connections Between the CPLD and Other XSB Board Components

CPLD Pin	CPLD Pin Function	Net Name	FPGA Pin	Parallel Port	Flash	SRAM	SDRAM	Stereo Codec	Ether-net	USB	IDE Intfc.	Cmpct. Flash	Switch Button	LEDs	JP7	Prog. Osc.
1		PB-A0	83		A0	A0	A0		SA0	FIFOADR0	DA0	A00		BAR1	23	
2		PB-D0	153		D0	D0	D0	CCLK	D0	FD0	DD0	D00		LEFT-A	7	
3	VCCINT															
4		PB-D1	145		D1	D1	D1	CDTI	D1	FD1	DD1	D01		LEFT-B	8	
5		PB-D2	141		D2	D2	D2	CDTO	D2	FD2	DD2	D02		LEFT-C	9	
6		PB-D3	135		D3	D3	D3		D3	FD3	DD3	D03		LEFT-D	10	
7		PB-D4	126		D4	D4	D4		D4	FD4	DD4	D04		LEFT-E	11	
8		PB-D5	120		D5	D5	D5		D5	FD5	DD5	D05		LEFT-F	12	
9		PB-D6	116		D6	D6	D6		D6	FD6	DD6	D06		LEFT-G	13	
10		PB-D7	108		D7	D7	D7		D7	FD7	DD7	D07		LEFT-DP	14	
11		FLASH-CE#	57		CE#											
12		PB-OE#	125		OE#	OE#	OE#		IORD#	SLOE		OE#/OE#/ATA_SEL#			3	
13		FPGA-TCK	207													
14	GND															
15	GCK1	FPGA-CS#/TDI	159													
15	GCK1	FPGA-CS#/TDI	160													
16	GCK2	FPGA-CCLK	155													
17	GCK3	CPLD-CLK														XBUF
18		FPGA-BSY/DOUT/TMS	2													
18		FPGA-BSY/DOUT/TMS	154													
19		FPGA-WRITE#/TDO	157													
19		FPGA-WRITE#/TDO	161													
20		PP-S4		S4												
21	GND															
22		PP-D7		D7												
23		PP-D6		D6												
24		PP-D5		D5												
25		PP-D4		D4												
26	VCCIO															
27		PP-D3		D3												
28	TDI	PP-C3		C3												
29	TMS	PP-C2		C2												
30	TCK	PP-C1#		C1#												
31		PP-D2		D2												
32		PP-D1		D1												
33		PP-D0		D0												
34		PP-S3		S3												
35		PP-S5		S5												
36		FPGA-M0	52													
37	VCCINT															
38		FPGA-INIT#	107													
39		FPGA-PROGRAM#	106										S7			
40		FPGA-DONE	104													
41	GND															
42		PB-A18	121		A18					SLRD	DIOR#	IORD#	S5-7		41	
43		PB-A11	109		A11	A11	A11						S4		34	
44		PB-A9	101		A9	A9	A9		SA9			A09	S2		32	
45		PB-A8	100		A8	A8	A8		SA8			A08	S1		31	
46		PB-A13	111		A13	A13	BA0						S5-2		36	
47		PB-A14	112		A14	A14	BA1						S5-3		37	
48		PB-A17	115		A17	A17				PKTEND		REG#	S5-6		40	
49		PB-WE#	123		WE#	WE#	WE#		IOWR#			WE#			4	
50		PB-A19	122							SLWR	DIOW#	IOWR#	S5-8		42	
51		PB-A16	114		A16	A16							S5-5		39	
52		PB-A15	113		A15	A15							S5-4		38	
53	TDO			S7#												
54	GND															
55	VCCIO															
56		PB-A12	110		A12	A12	A12						S5-1		35	
57		PB-A10	102		A10	A10	A10					A10	S3		33	
58		PB-A7	94		A7	A7	A7		SA7			A07		BAR8	30	
59		PB-A6	93		A6	A6	A6		SA6			A06		BAR7	29	
60		PB-A5	89		A5	A5	A5		SA5			A05		BAR6	28	
61		PB-A4	88		A4	A4	A4		SA4			A04		BAR5	27	
62		PB-A3	87		A3	A3	A3		SA3			A03		BAR4	26	
63		PB-A2	86		A2	A2	A2		SA2	FIFOADR2	DA2	A02		BAR3	25	
64		PB-A1	84		A1	A1	A1		SA1	FIFOADR1	DA1	A01		BAR2	24	

B

XSB Schematics

The following pages show the detailed schematics for the XSB Board.


U1B7
ADC-CLK
ADC-OE#
I2C-SDA
I2C-SCL
VIDOUT-VSYNC#
VIDOUT-HSYNC#
VIDOUT-GY0
VIDOUT-GY1
VIDOUT-GY2
VIDOUT-GY3
VIDOUT-GY4
VIDOUT-GY5
VIDOUT-GY6
VIDOUT-GY7
VIDOUT-GY8
VIDOUT-GY9
VIDOUT-CLK
VIDOUT-BLANK#
IO_B7_0
IO_B7_1
IO_B7_2
IO_B7_3_(VREF,L49P)
IO_B7_4_(L49N)
IO_B7_5
IO_B7_6
IO_B7_7_(L48P)
IO_B7_8_(L48N)
IO_B7_9_(L47P_YY)
IO_B7_10_(L47N_YY)
IO_B7_11_(L46P_YY)
IO_B7_12_(L46N_YY)
IO_B7_13_(VREF,L45P)
IO_B7_14_(L45N)
IO_B7_15
IO_B7_16_(L44P_YY)
IO_B7_17_(IRDY,L44N_YY)
R52F 33
XC2S300E_PQ208
U1B6
VIDOUT-RCR9
VIDOUT-RCR8
VIDOUT-RCR7
VIDOUT-RCR6
VIDOUT-RCR5
VIDOUT-RCR4
VIDOUT-RCR3
VIDOUT-RCR2
VIDOUT-RCR1
VIDOUT-RCR0
VIDOUT-BCB0
VIDOUT-BCB1
VIDOUT-BCB2
VIDOUT-BCB3
VIDOUT-BCB4
VIDOUT-BCB5
VIDOUT-BCB6
VIDOUT-BCB7
IO_B6_0_(TRDY)
IO_B6_1
IO_B6_2_(L43P)
IO_B6_3_(VREF,L43N)
IO_B6_4_(L42P_YY)
IO_B6_5_(L42N_YY)
IO_B6_6_(L41P_YY)
IO_B6_7_(L41N_YY)
IO_B6_8_(L40P)
IO_B6_9_(L40N)
IO_B6_10
IO_B6_11
IO_B6_12
IO_B6_13_(VREF,L39P)
IO_B6_14_(L39N)
IO_B6_15
IO_B6_16_(L38P_YY)
IO_B6_17_(L38N_YY)
R54H 33
XC2S300E_PQ208
U1B5
VIDOUT-BCB8
VIDOUT-BCB9
FLASH-CE#
PB-ECS0#
NV-CS0#
NV-CS1#
NV-INTRQ
NV-IORDY
NV-IOCS16
NV-DMACK#
NV-DMARQ
RS232-CTS
RS232-RTS
RS232-TD
RS232-RD
ETHERNET-IOCS16#
ETHERNET-IREQ
IO_B5_0_(L37N_YY)
IO_B5_1_(L37P_YY)
IO_B5_2
IO_B5_3
IO_B5_4_(VREF,L36N_YY)
IO_B5_5_(L36P_YY)
IO_B5_6_(L35N)
IO_B5_7_(L35P)
IO_B5_8_(L34N)
IO_B5_9_(L34P)
IO_B5_10_(L33N)
IO_B5_11_(L33P)
IO_B5_12
IO_B5_13_(L32N)
IO_B5_14_(VREF,L32P)
IO_B5_15
IO_B5_16_(DLL,L31N)
XC2S300E_PQ208
+3.3V
R70A 4.7K
U1B4
ETHERNET-RDY/DTACK
ETHERNET-CS#
PB-A0
PB-A1
PB-A2
PB-A3
PB-A4
PB-A5
PB-A6
PB-A7
SDRAM-WE#
SDRAM-CAS#
SDRAM-RAS#
SDRAM-CE#
SDRAM-CKE
PB-A8
PB-A9
PB-A10
IO_B4_0_(DLL,L31P)
IO_B4_1
IO_B4_2_(L30N)
IO_B4_3_(VREF,L30P)
IO_B4_4_(L29N)
IO_B4_5_(L29P)
IO_B4_6_(L28N)
IO_B4_7_(L28P)
IO_B4_8_(L27N_YY)
IO_B4_9_(L27P_YY)
IO_B4_10
IO_B4_11
IO_B4_12_(L26N_YY)
IO_B4_13_(VREF,L26P_YY)
IO_B4_14
IO_B4_15
IO_B4_16_(L25N_YY)
IO_B4_17_(L25P_YY)
R52H 33
R58C 33
XC2S300E_PQ208
U1B3
FPGA-INIT#
PB-D7
PB-A11
PB-A12
PB-A13
PB-A14
PB-A15
PB-A16
PB-A17
PB-D6
PB-D5
PB-A18
PB-A19
PB-WE#
PB-OE#
PB-D4
PB-D8
PB-D9
IO_B3_0_(INIT#,L24N_YY)
IO_B3_1_(D7,L24P_YY)
IO_B3_2
IO_B3_3
IO_B3_4_(VREF,L23N)
IO_B3_5_(L23P)
IO_B3_6
IO_B3_7
IO_B3_8_(L22N)
IO_B3_9_(D6,L22P)
IO_B3_10_(D5,L21N_YY)
IO_B3_11_(L21P_YY)
IO_B3_12_(L20N_YY)
IO_B3_13_(L20P_YY)
IO_B3_14_(VREF,L19N)
IO_B3_15_(D4,L19P)
IO_B3_16
IO_B3_17_(TRDY)
R60D 33
XC2S300E_PQ208
U1B2
PB-D10
PB-D11
PB-D12
PB-D3
PB-D13
PB-D14
PB-D15
PB-LB#
PB-D2
PB-D1
PB-UB#
RAM-CE#
USB-CS#
USB-INT#
USB-READY
USB-FLAGC
USB-FLAGB
PB-D0
FPGA-BSY/DOUT/TMS
IO_B2_0_(IRDY,L18N_YY)
IO_B2_1_(L18P_YY)
IO_B2_2
IO_B2_3_(D3,L17N)
IO_B2_4_(VREF,L17P)
IO_B2_5_(L16N_YY)
IO_B2_6_(L16P_YY)
IO_B2_7_(L15N_YY)
IO_B2_8_(D2,L15P_YY)
IO_B2_9_(D1,L14N)
IO_B2_10_(L14P)
IO_B2_11
IO_B2_12
IO_B2_13
IO_B2_14_(VREF,L13N)
IO_B2_15_(L13P)
IO_B2_16
IO_B2_17_(DIN/D0,L12N_YY)
IO_B2_18_(DOUT/BUSY,L12P_YY)
R61H 33
XC2S300E_PQ208
+3.3V
+3.3V
R70C 4.7K
R70B 4.7K
U1CONFIG
FPGA-DONE
FPGA-PROGRAM#
FPGA-CCLK
FPGA-M0
+3.3V
GND
FPGA-TCK
FPGA-BSY/DOUT/TMS
FPGA-CS#/TDI
FPGA-WRITE#/TDO
SDRAM-CLK
FPGA-CLK1
FPGA-CLK0
VIDIN-ICLK
DONE
PROGRAM#
CCLK
M0
M1
M2
TCK
TMS
TDI
TDO
I/GCK0
I/GCK1
I/GCK2
I/GCK3
R69B 330
XC2S300E_PQ208
U1B1
FPGA-CS#/TDI
FPGA-WRITE#/TDO
USB-FLAGA
USB-IFCLK
USB-VBUS
AU-CSN#
AU-BCLK
AU-MCLK
AU-LRCK
AU-SDTI
AU-SDTO0
VIDIN-HPD0
VIDIN-HPD1
VIDIN-HPD2
VIDIN-HPD3
VIDIN-HPD4
VIDIN-HPD5
VIDIN-HPD6
IO_B1_0_(CS#,L11P_YY)
IO_B1_1_(WRITE#,L11N_YY)
IO_B1_2
IO_B1_3
IO_B1_4_(VREF,L10P_YY)
IO_B1_5_(L10N_YY)
IO_B1_6
IO_B1_7
IO_B1_8_(L9P)
IO_B1_9_(L9N)
IO_B1_10_(L8P)
IO_B1_11_(L8N)
IO_B1_12_(L7P)
IO_B1_13_(L7N)
IO_B1_14_(VREF,L6P)
IO_B1_15_(L6N)
IO_B1_16
IO_B1_17_(DLL,L5N)
XC2S300E_PQ208
U1B0
VIDIN-HPD7
VIDIN-IPD0
VIDIN-IPD1
VIDIN-IPD2
VIDIN-IPD3
VIDIN-IPD4
VIDIN-IPD5
VIDIN-IPD6
VIDIN-IPD7
VIDIN-IGPH
VIDIN-IGPV
VIDIN-IGP1
VIDIN-IGP0
VIDIN-ITRI
VIDIN-IDQ
VIDIN-ITRDY
IO_B0_0_(DLL,L5N)
IO_B0_1_(L4P)
IO_B0_2_(VREF,L4N)
IO_B0_3_(L3P)
IO_B0_4_(L3N)
IO_B0_5_(L2P)
IO_B0_6_(L2N)
IO_B0_7_(L1P_YY)
IO_B0_8_(L1N_YY)
IO_B0_9
IO_B0_10
IO_B0_11_(L0P_YY)
IO_B0_12_(VREF,L0N_YY)
IO_B0_13
IO_B0_14
IO_B0_15
XC2S300E_PQ208
R70D 4.7K
R69D 330
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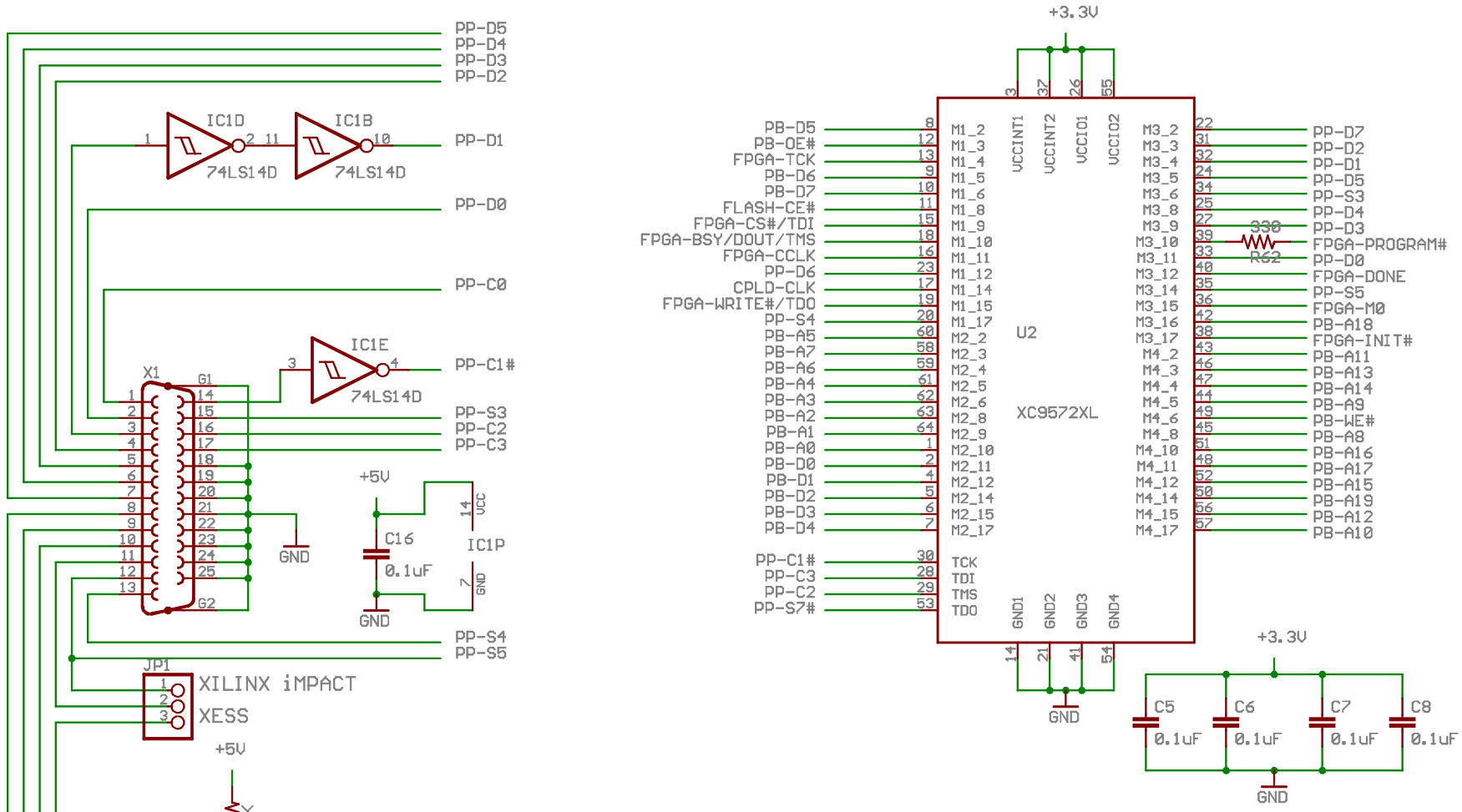
Sheet: 1/16



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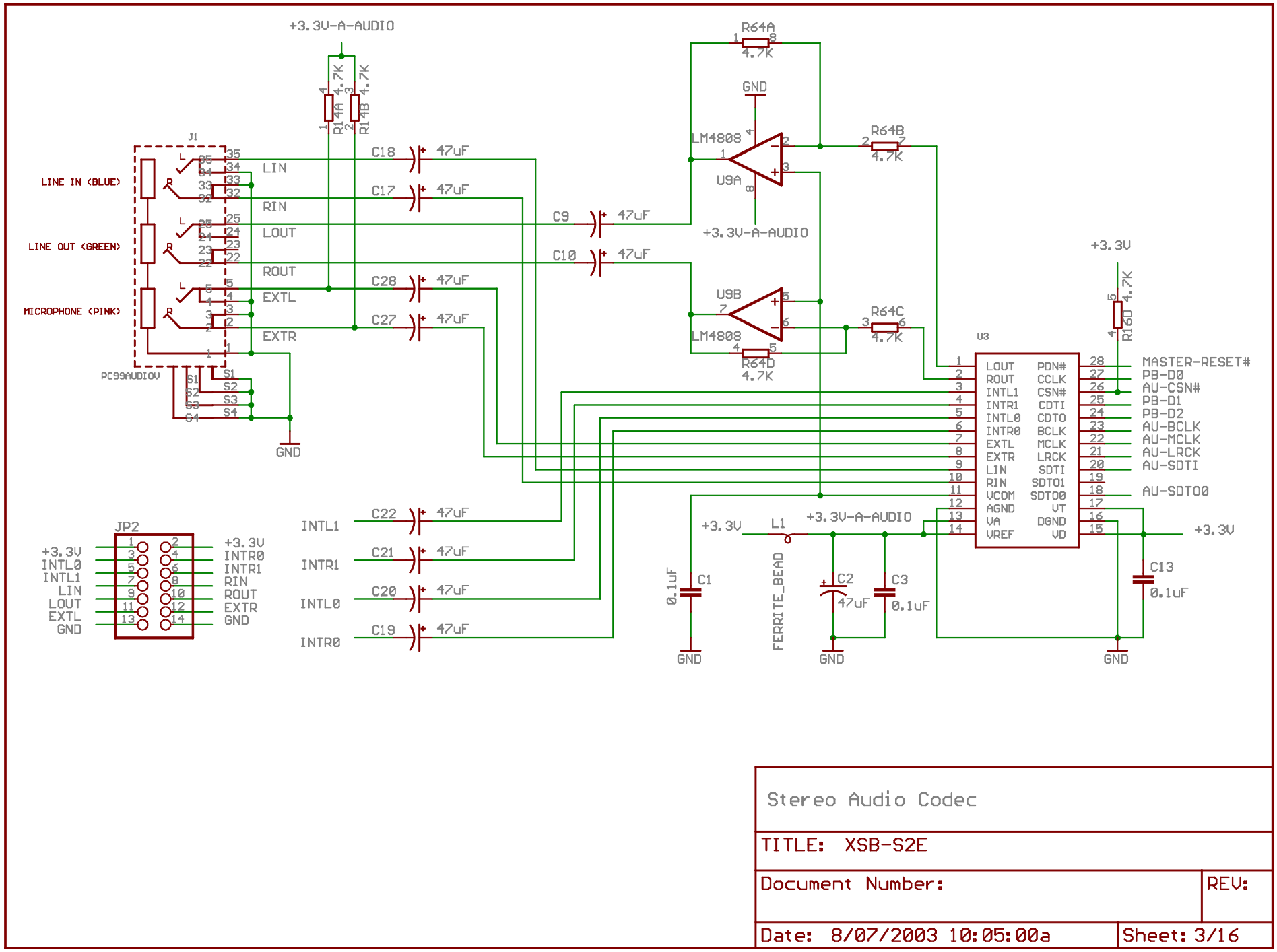

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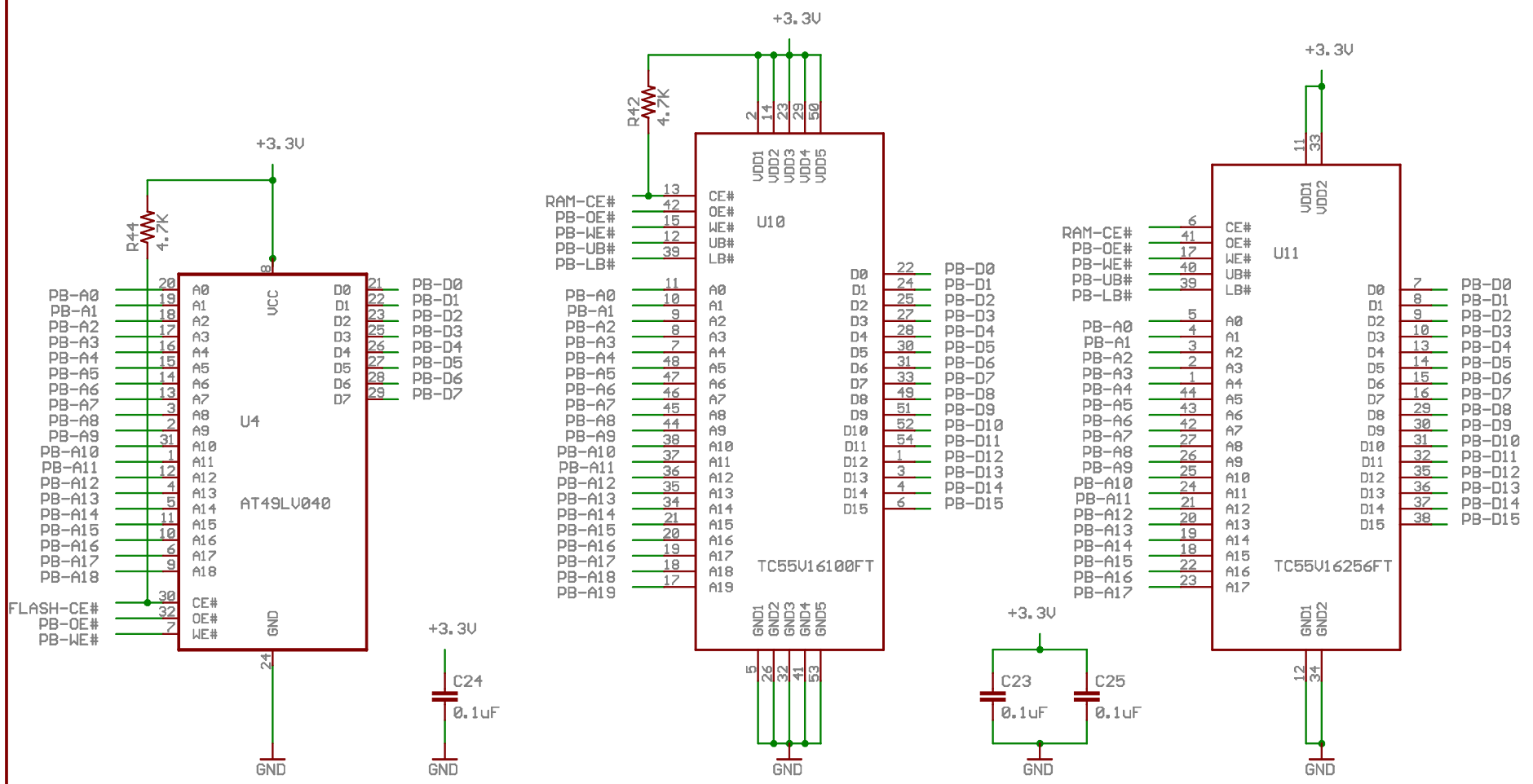

Flash and Static RAMs

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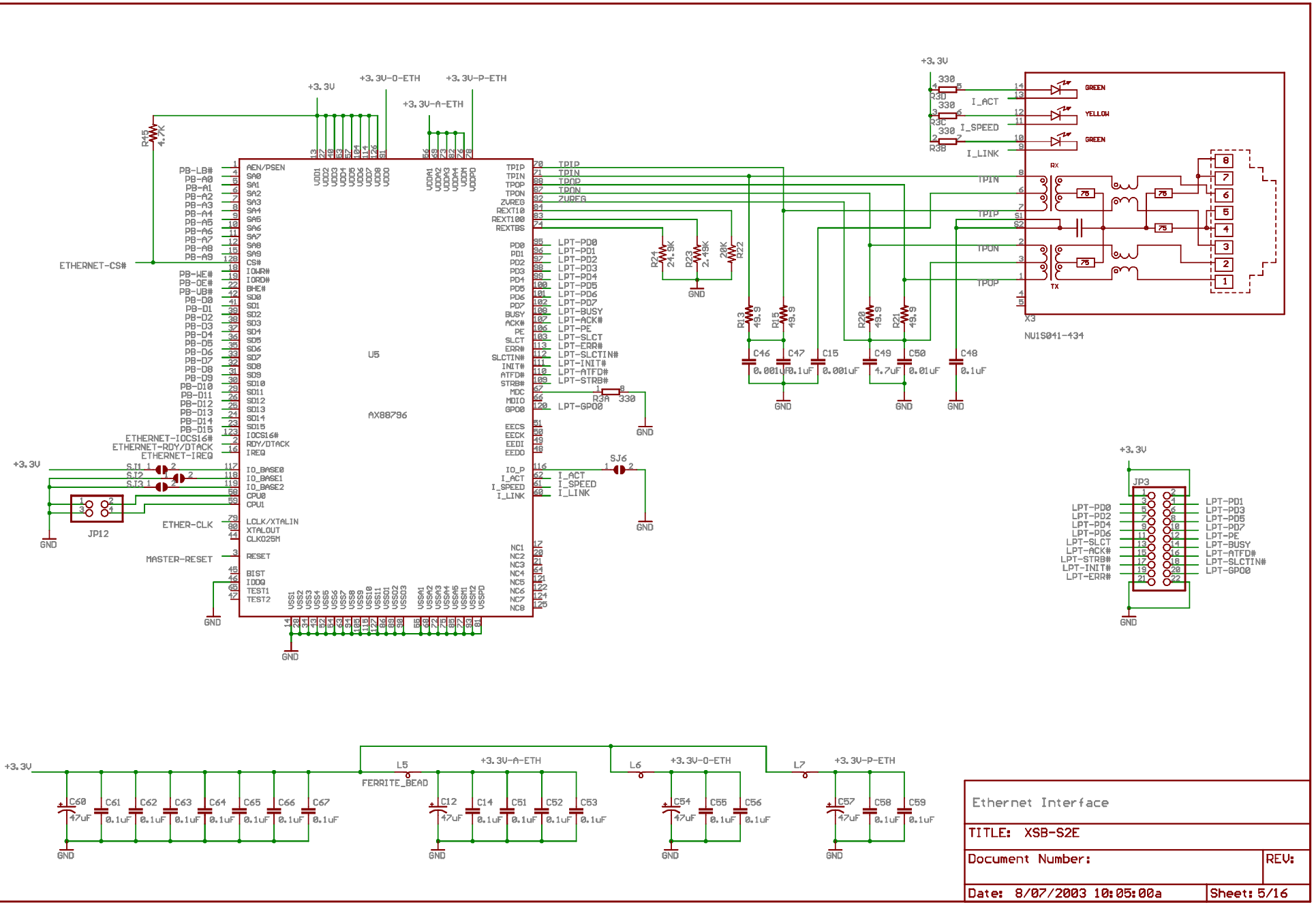

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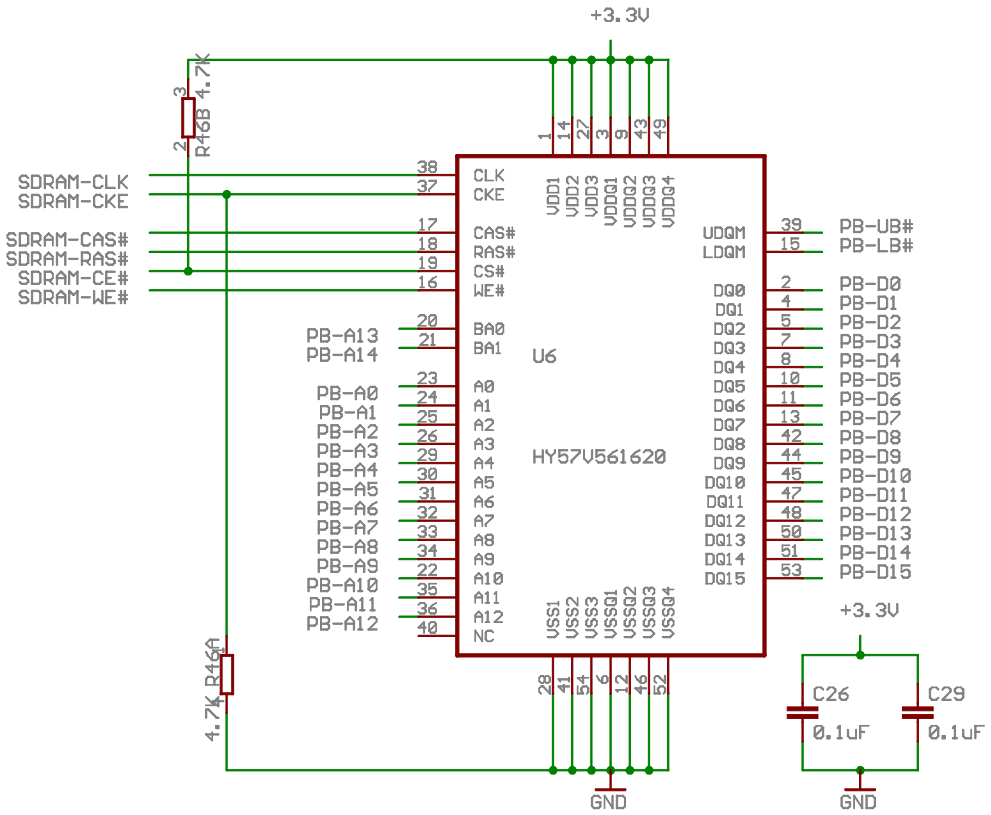

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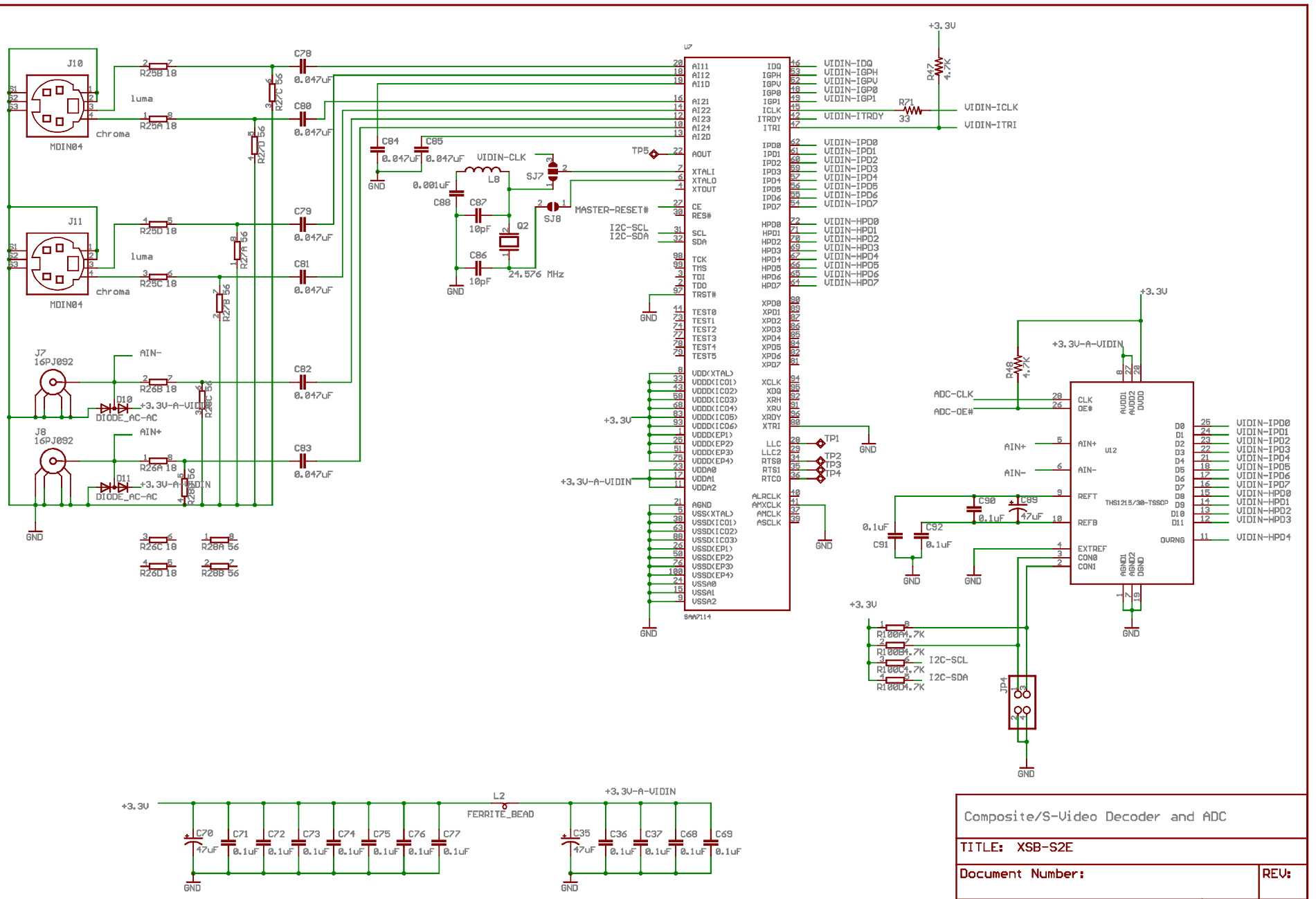
J10
MDIN04
luma
chroma
J11
MDIN04
luma
chroma
J7
16PJ092
AIN-
D10
DIODE_AC-AC
+3.3V-A-VIDIN
J8
16PJ092
AIN+
D11
DIODE_AC-AC
+3.3V-A-VIDIN
R25B 18
R25A 18
R25D 18
R25C 18
R26B 18
R26A 18
R26C 18
R26D 18
R27C 56
R27D 56
R27A 56
R27B 56
R28C 56
R28D 56
R28A 56
R28B 56
C78
C80
C79
C81
C82
C83
0.047uF
GND
U7
SAA7114
C84
C85
0.047uF
0.047uF
VIDIN-CLK
L8
0.001uF
C88
C87
10pF
Q2
C86
10pF
24.576 MHz
SJ7
SJ8
MASTER-RESET#
I2C-SCL
I2C-SDA
TP5
TP1
TP2
TP3
TP4
+3.3V
+3.3V-A-VIDIN
VIDIN-IDQ
VIDIN-IGPH
VIDIN-IGPV
VIDIN-IGP0
VIDIN-IGP1
VIDIN-ITRDY
VIDIN-IPD0
VIDIN-IPD1
VIDIN-IPD2
VIDIN-IPD3
VIDIN-IPD4
VIDIN-IPD5
VIDIN-IPD6
VIDIN-IPD7
VIDIN-HPD0
VIDIN-HPD1
VIDIN-HPD2
VIDIN-HPD3
VIDIN-HPD4
VIDIN-HPD5
VIDIN-HPD6
VIDIN-HPD7
R47 4.7K
R71 33
VIDIN-ICLK
VIDIN-ITRI
+3.3V
+3.3V-A-VIDIN
R48 4.7K
ADC-CLK
ADC-OE#
AIN+
AIN-
C90
C89
47uF
0.1uF
C91
C92
0.1uF
0.1uF
REFT
REFB
EXTREF
CON0
CON1
THS1215/30-TSSOP
U12
VIDIN-IPD0
VIDIN-IPD1
VIDIN-IPD2
VIDIN-IPD3
VIDIN-IPD4
VIDIN-IPD5
VIDIN-IPD6
VIDIN-IPD7
VIDIN-HPD0
VIDIN-HPD1
VIDIN-HPD2
VIDIN-HPD3
VIDIN-HPD4
+3.3V
R100A 4.7K
R100B 4.7K
R100C 4.7K
R100D 4.7K
I2C-SCL
I2C-SDA
JP4
GND
+3.3V
L2
FERRITE_BEAD
+3.3V-A-VIDIN
C70
C71
C72
C73
C74
C75
C76
C77
C35
C36
C37
C68
C69
47uF
0.1uF
GND
Composite/S-Video Decoder and ADC
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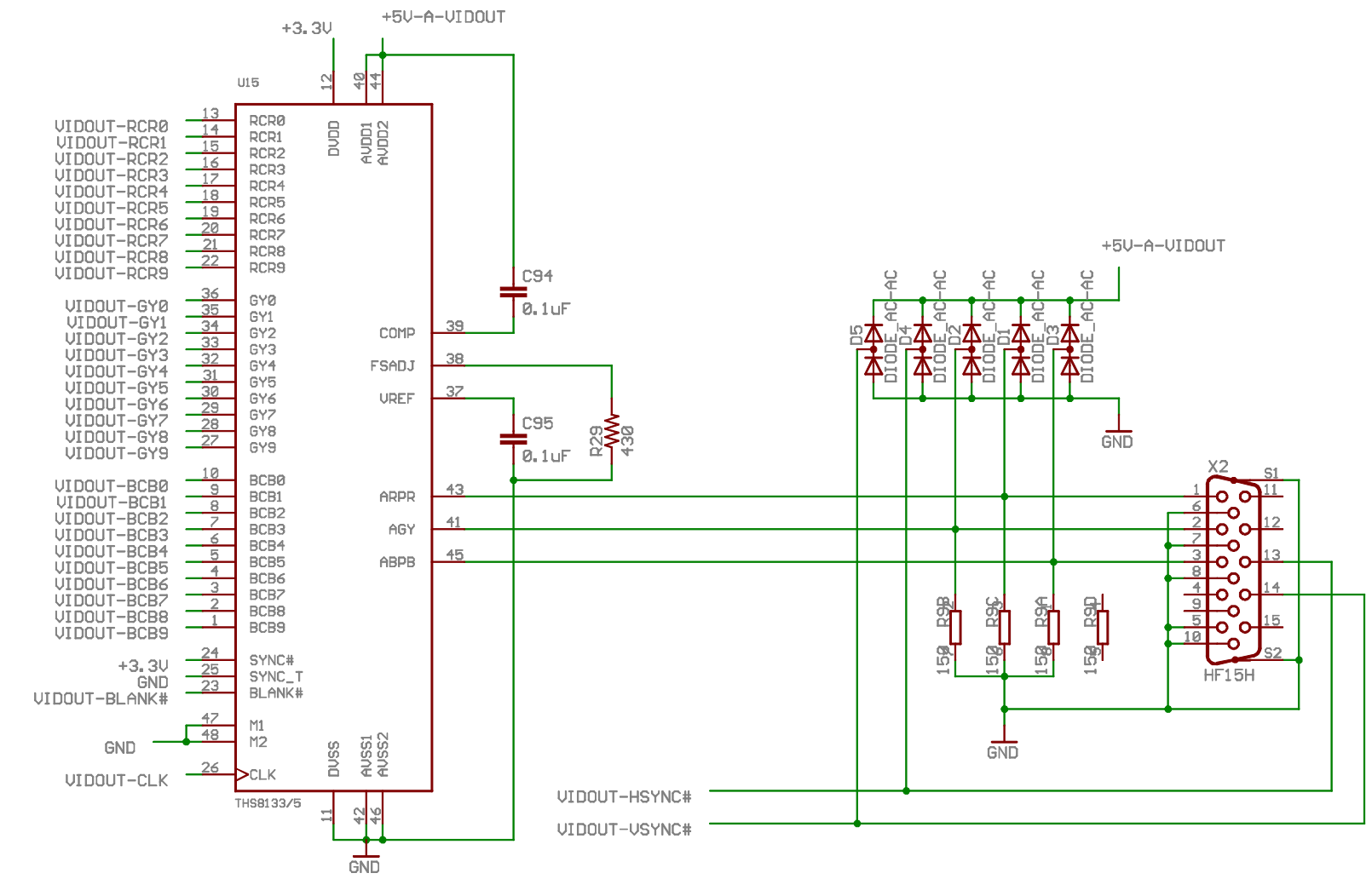
Date: 8/07/2003 10:05:00a
Sheet: 7/16



VGA Video Output

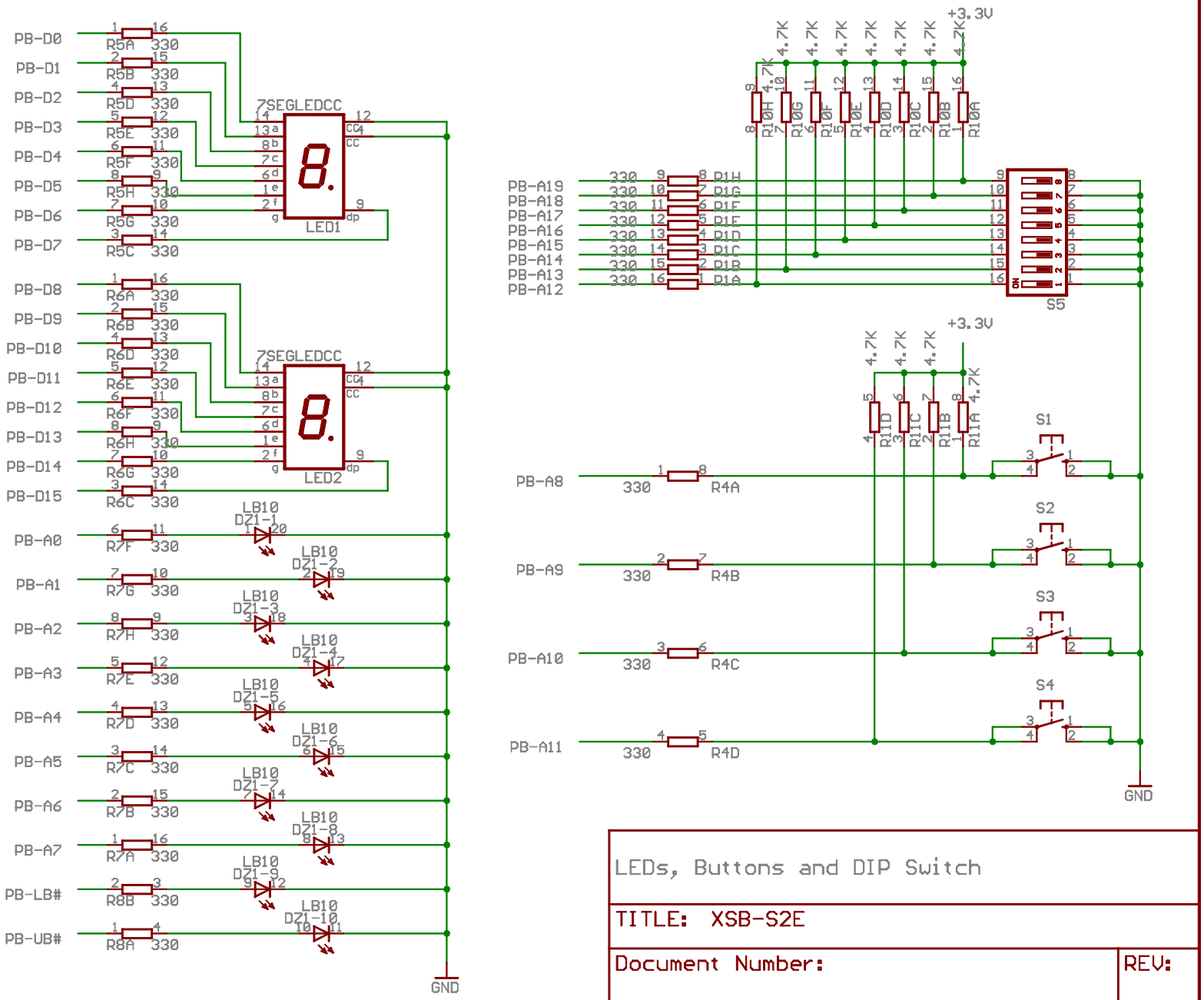
TITLE: XSB-S2E

Document Number:

REV:

Date: 8/07/2003 10:05:00a

Sheet: 8/16



LEDs, Buttons and DIP Switch

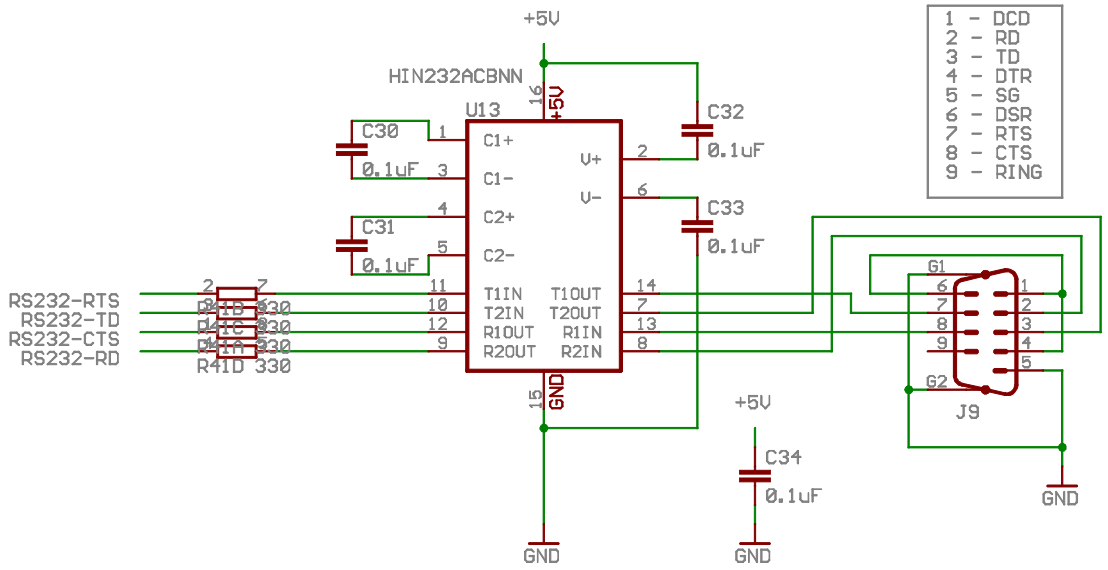
TITLE: XSB-S2E

Document Number:

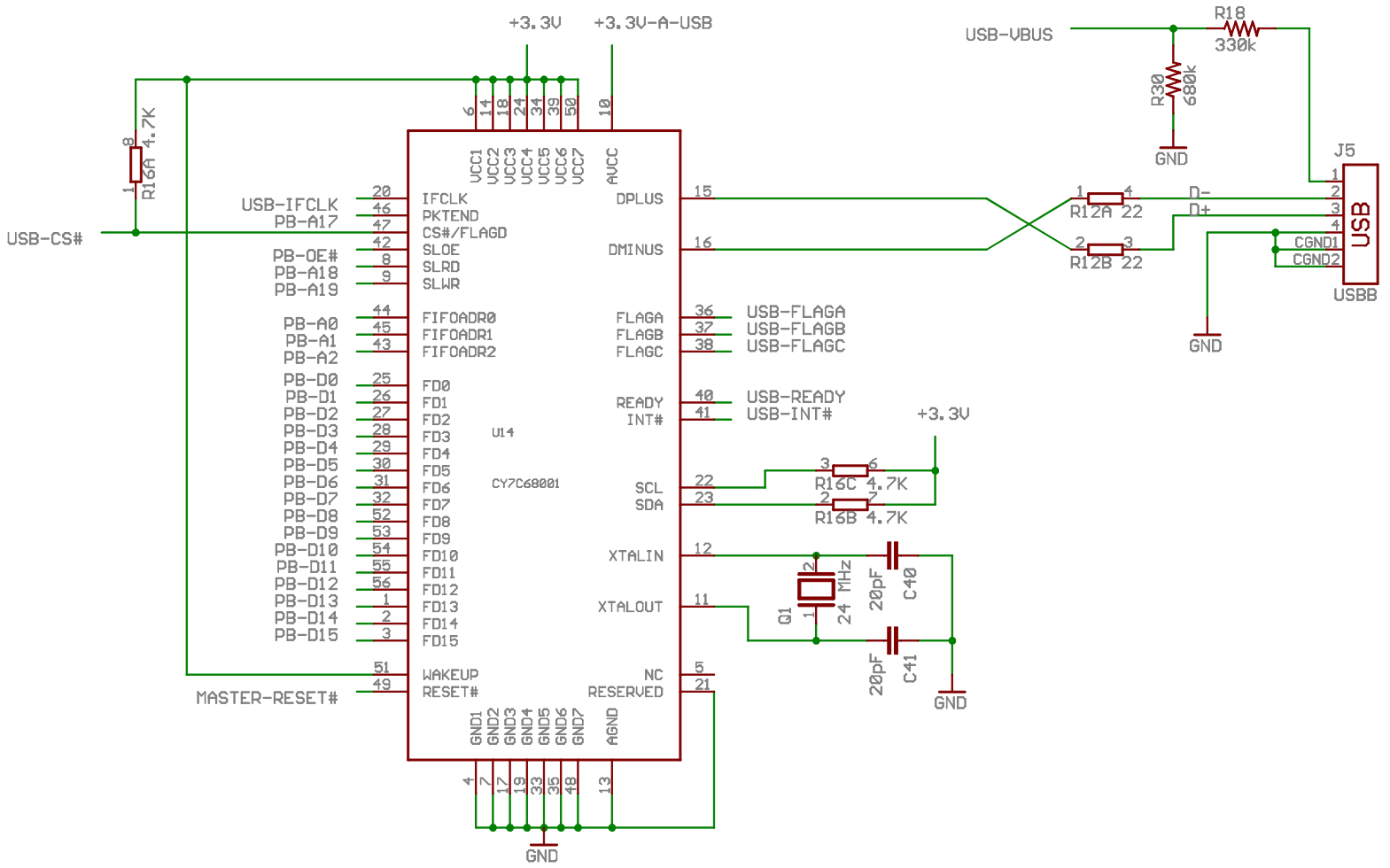
REV:

Date: 8/07/2003 10:05:00a

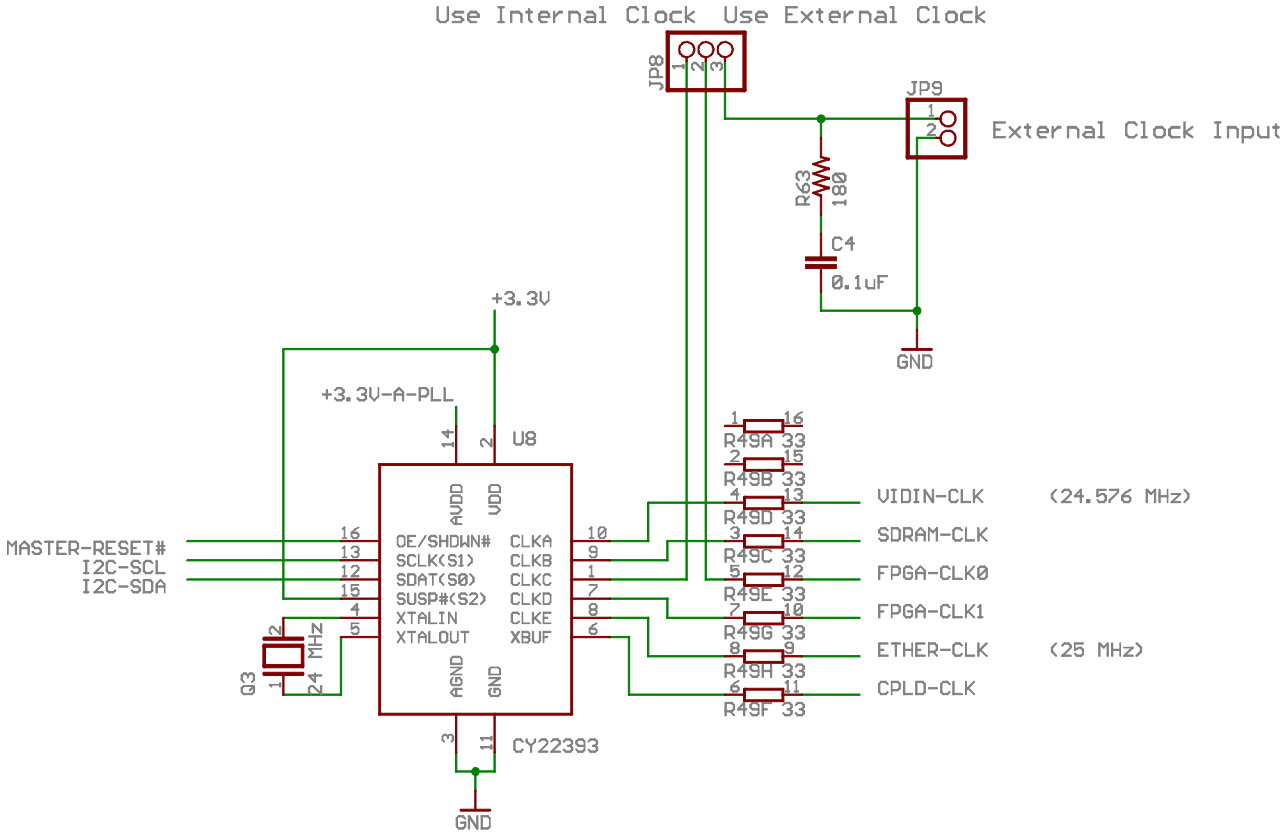
Sheet: 9/16

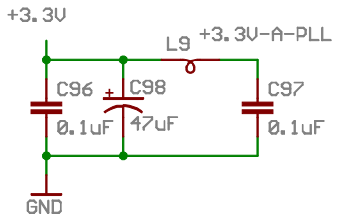


RS-232 Serial Interface		
TITLE: XSB-S2E		
Document Number:		REV:
Date: 8/07/2003 10:05:00a	Sheet: 10/16	

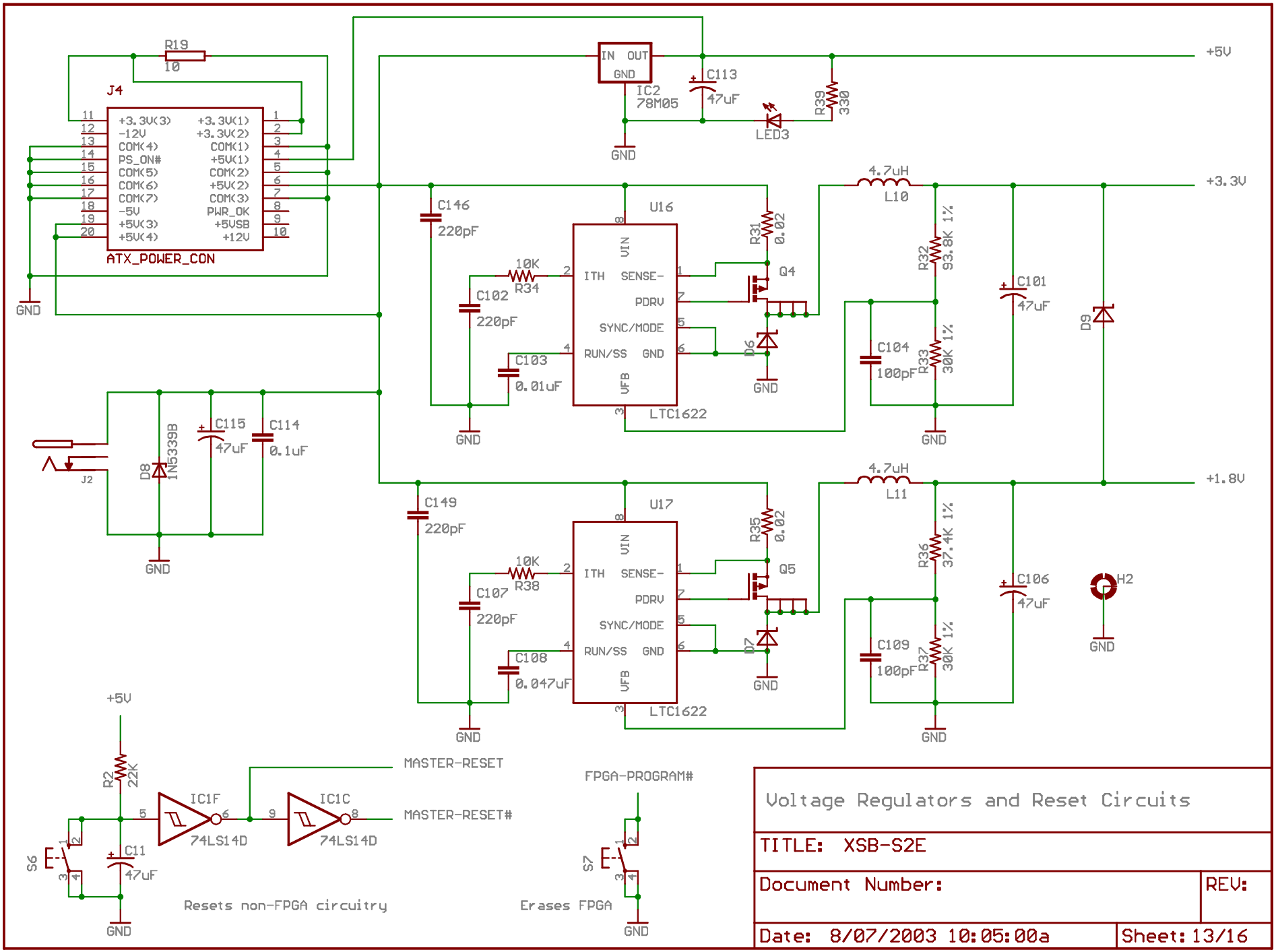


USB 2.0 Interface	
TITLE: XSB-S2E	
Document Number:	REV:
Date: 8/07/2003 10:05:00a	Sheet: 11/16





Clock Generator	
TITLE: XSB-S2E	
Document Number:	REV:
Date: 8/07/2003 10:05:00a	Sheet: 12/16


R19
10
J4
+3.3V(3)
-12V
COM(4)
PS_ON#
COM(5)
COM(6)
COM(7)
-5V
+5V(3)
+5V(4)
+3.3V(1)
+3.3V(2)
COM(1)
+5V(1)
COM(2)
+5V(2)
COM(3)
PWR_OK
+5VSB
+12V
ATX_POWER_CON
GND
IN OUT
GND
IC2
78M05
C113
47uF
LED3
R39
330
+5V
C146
220pF
U16
VIN
ITH
SENSE-
PDRV
SYNC/MODE
RUN/SS
GND
VFB
LTC1622
10K
R34
C102
220pF
C103
0.01uF
R31
0.02
Q4
D6
4.7uH
L10
R32
93.8K 1%
R33
30K 1%
C104
100pF
C101
47uF
D9
+3.3V
J2
D8
1N5339B
C115
47uF
C114
0.1uF
C149
220pF
U17
LTC1622
10K
R38
C107
220pF
C108
0.047uF
R35
0.02
Q5
D7
4.7uH
L11
R36
37.4K 1%
R37
30K 1%
C109
100pF
C106
47uF
H2
+1.8V
+5V
R2
22K
IC1F
74LS14D
IC1C
74LS14D
MASTER-RESET
MASTER-RESET#
S6
C11
47uF
Resets non-FPGA circuitry
FPGA-PROGRAM#
S7
Erases FPGA
Voltage Regulators and Reset Circuits
TITLE: XSB-S2E
Document Number:
REV:
Date: 8/07/2003 10:05:00a
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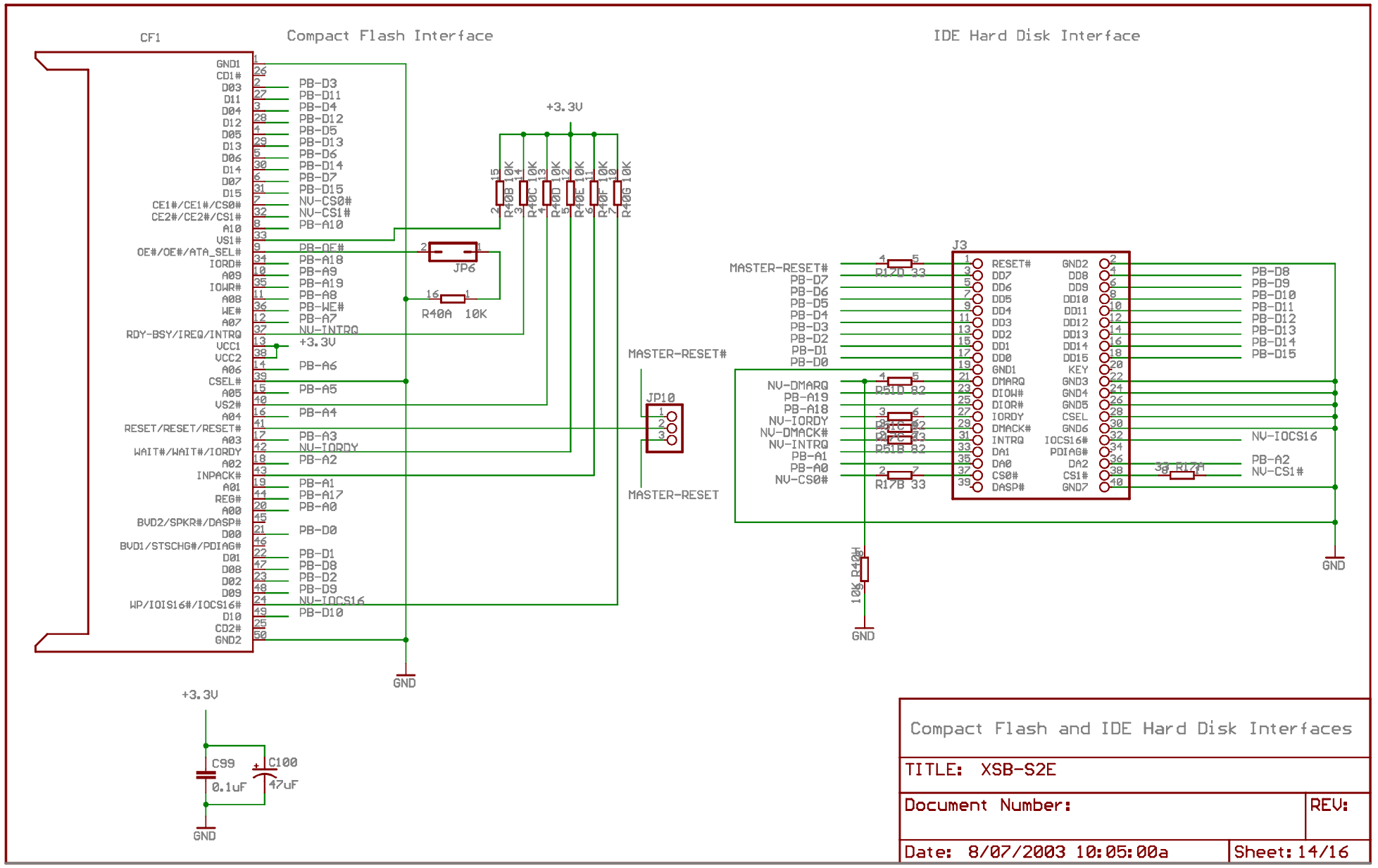
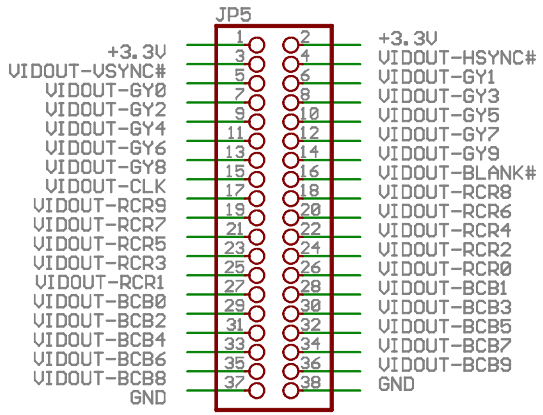
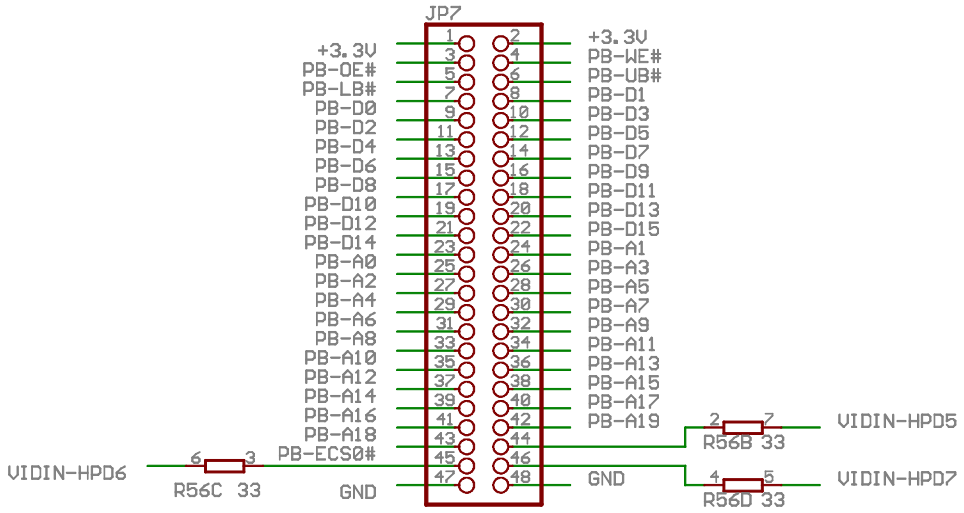


Compact Flash and IDE Hard Disk Interfaces	
TITLE: XSB-S2E	
Document Number:	REV:
Date: 8/07/2003 10:05:00a	Sheet: 14/16

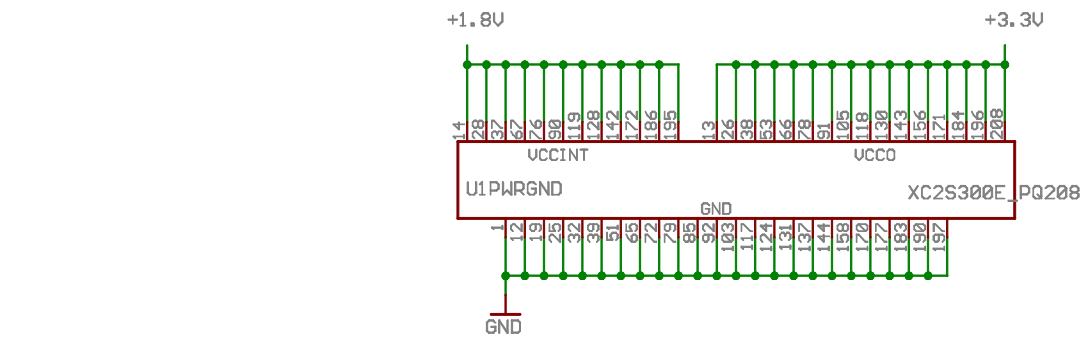
Expansion from Video Output

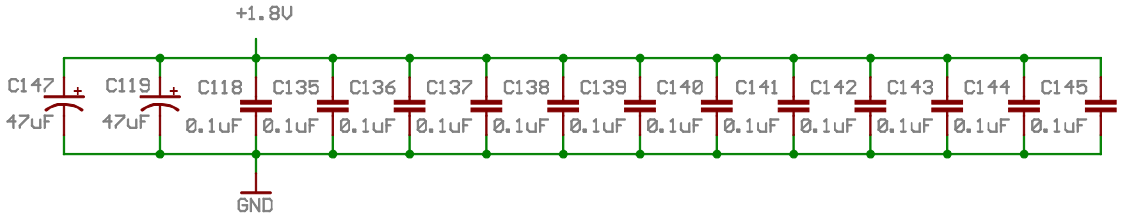


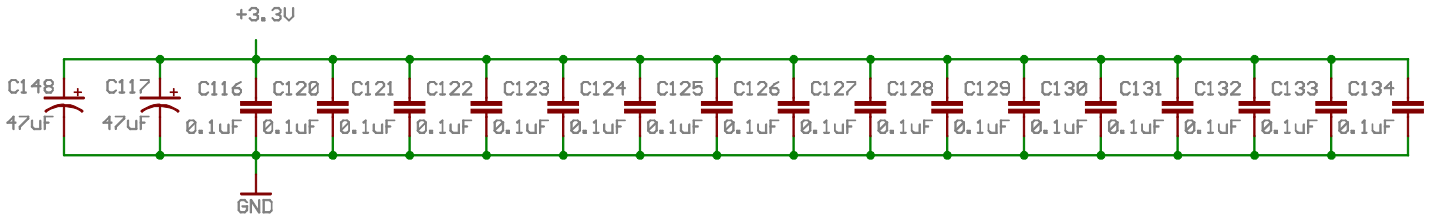
Expansion from Peripheral Bus



Expansion Connectors		
TITLE: XSB-S2E		
Document Number:		REV:
Date: 8/07/2003 10:05:00a	Sheet: 15/16	



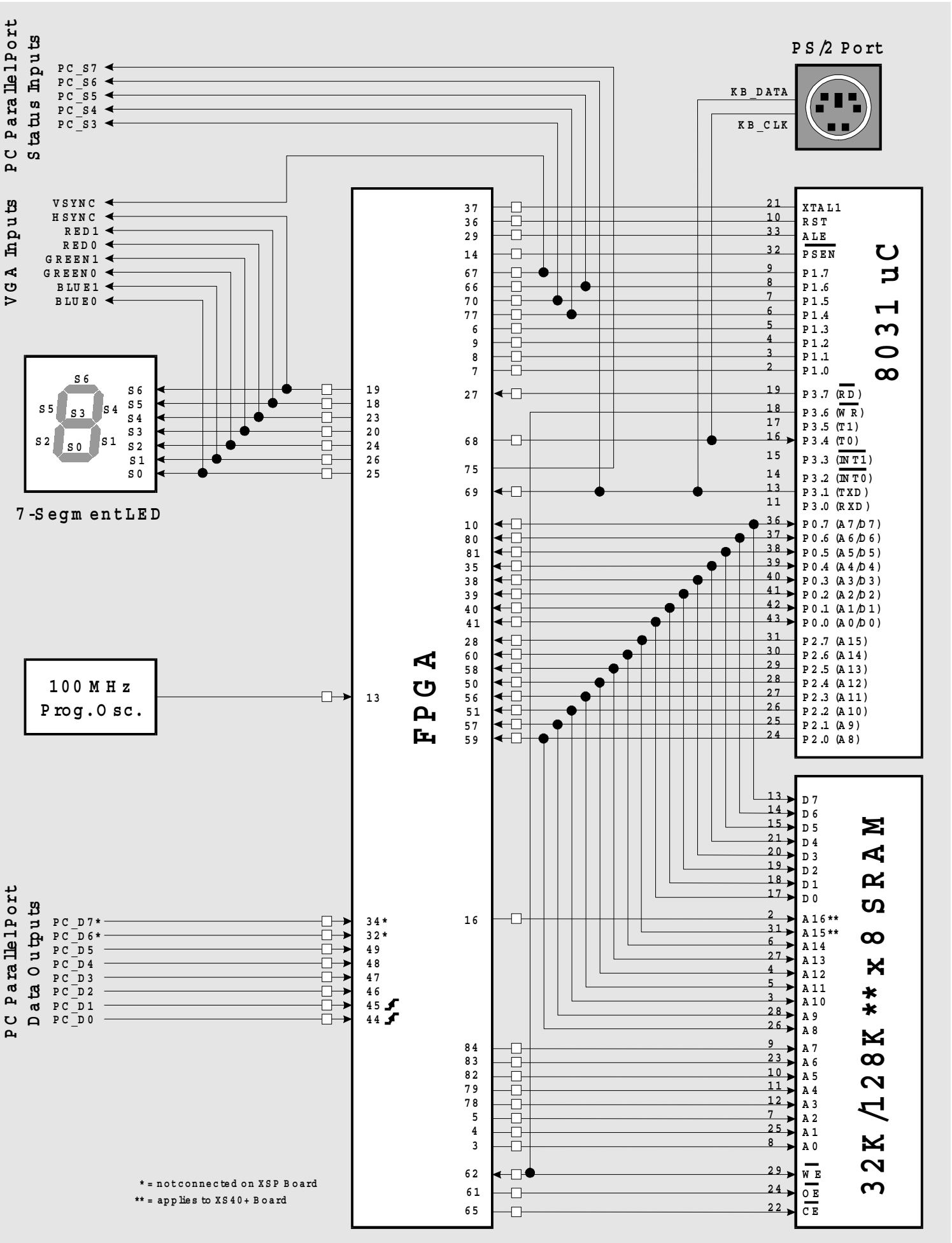


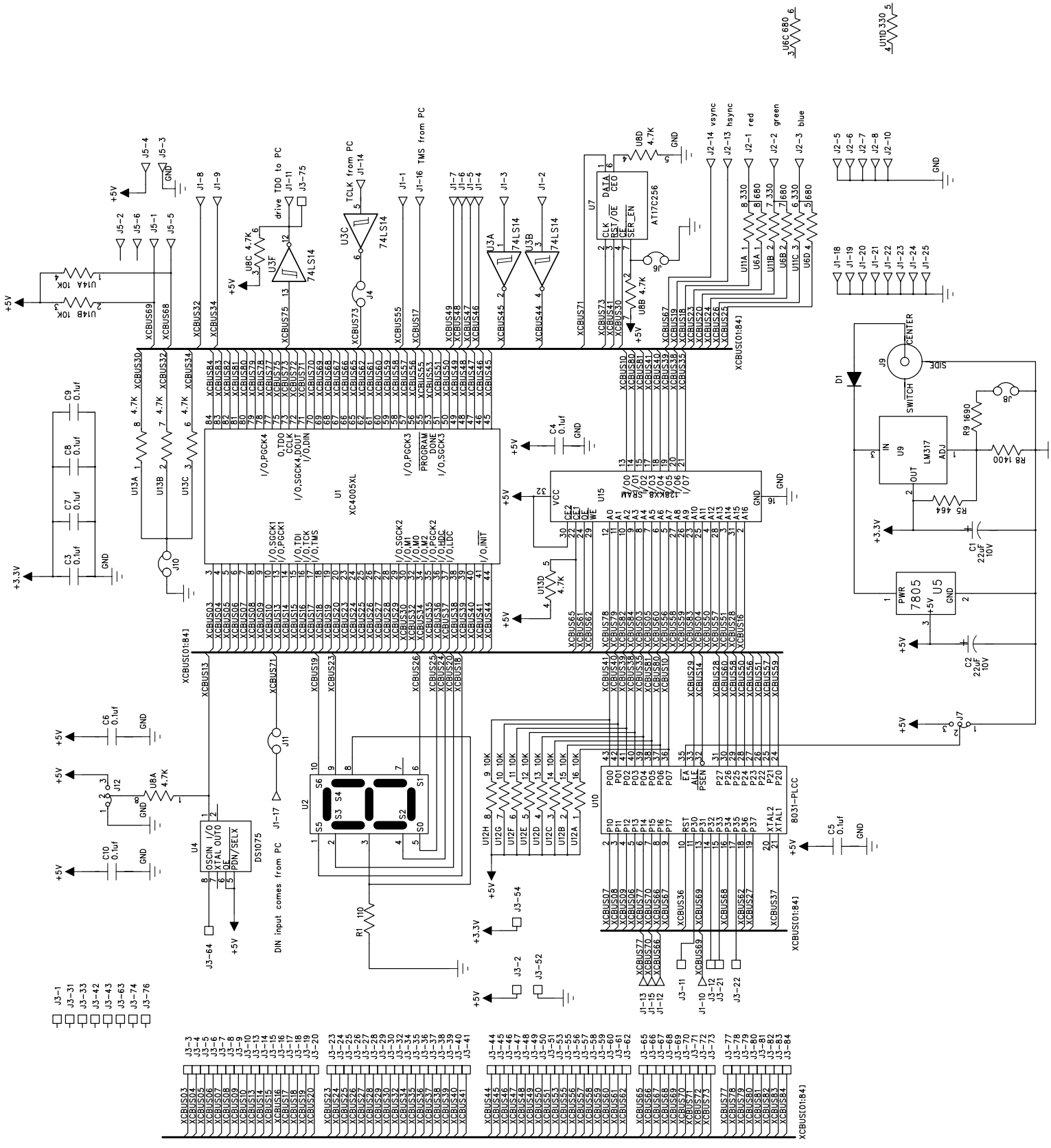


FPGA Bypass Capacitors		
TITLE: XSB-S2E		
Document Number:		REV:
Date: 8/07/2003 10:05:00a	Sheet: 16/16	

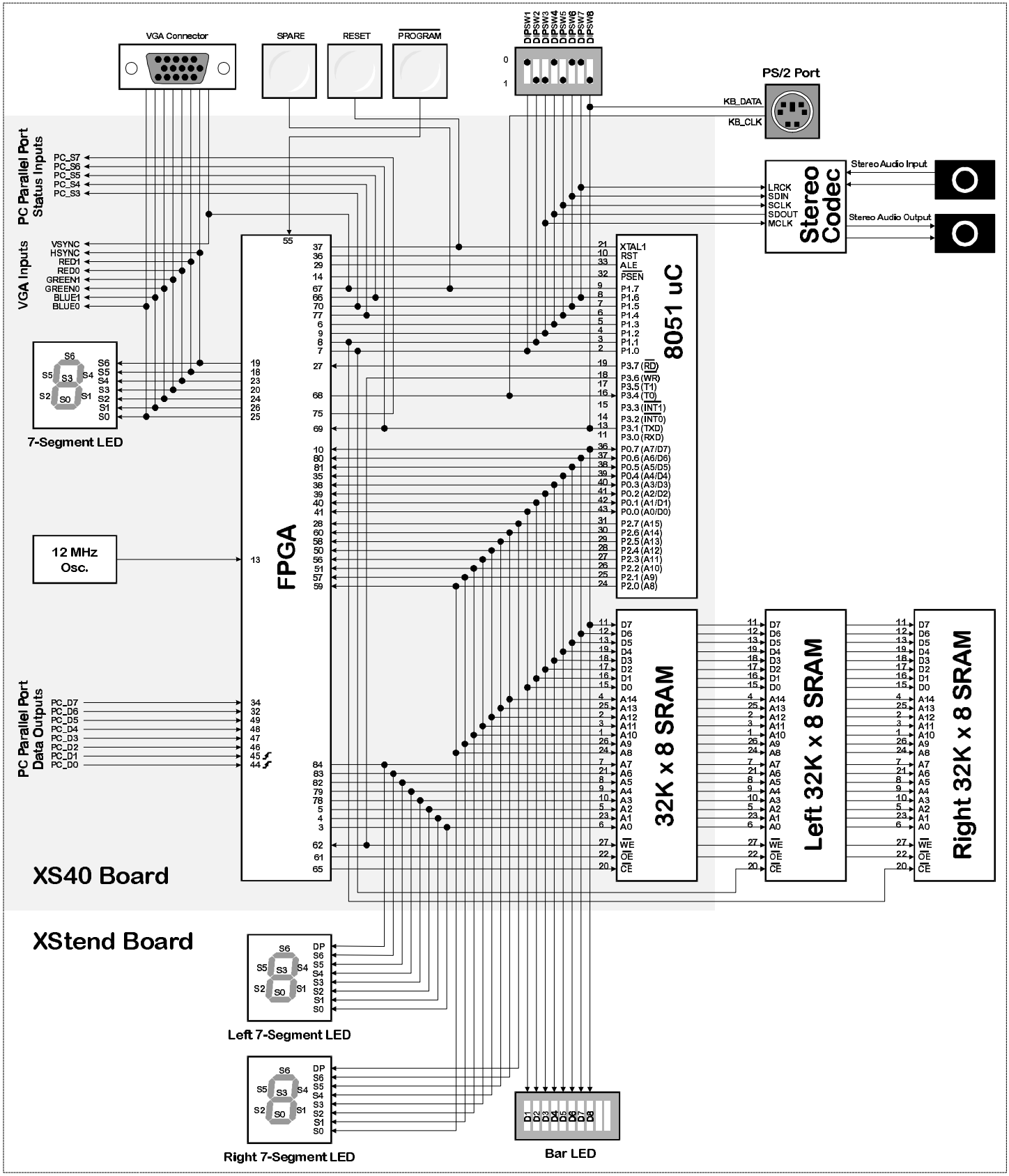
- Table 4: XS40 Board pin descriptions.

XS40 Pin	Connects to...	Description
25	S0_BLUE0	These pins drive the individual segments of the LED display (S0-S6). They also drive the color and horizontal sync signals for a VGA monitor.
26	S1_BLUE1	
24	S2_GREEN0	
20	S3_GREEN1	
23	S4_RED0	
18	S5_RED1	
19	S6_HSYNCB	
13	CLK	An input driven by the 100 MHz programmable oscillator
44	PC_D0	These pins are driven by the data output pins of the PC parallel port. Clocking signals can only be reliably applied through pins 44 and 45 since these have additional hysterisis circuitry. Pins 32 and 34 are mode signals for the FPGA so you must adjust your design to account for the way that the Foundation tools handle these pins. pins 32 and 34 are not usable as general-purpose I/O on the Spartan FPGA on the XSP Board.
45	PC_D1	
46	PC_D2	
47	PC_D3	
48	PC_D4	
49	PC_D5	
32	PC_D6	
34	PC_D7	
37	XTAL1	Pin that drives the uC clock input
36	RST	Pin that drives the uC reset input
29	ALER	Pin that monitors the uC address latch enable
14	PSENB	Pin that monitors the uC program store enable
7	P1.0	These pins connect to the pins of Port 1 of the uC. Some of the pins are also connected to the status input pins of the PC parallel port. Pin 67 drives the vertical sync signal for a VGA monitor.
8	P1.1	
9	P1.2	
6	P1.3	
77	P1.4_PC_S4	
70	P1.5_PC_S3	
66	P1.6_PC_S5	
67	P1.7_VSYNCB	
69	P3.1(TXD)_PC_S6	These pins connect to some of the pins of Port 3 of the uC. The uC has specialized functions for each of the port pins indicated in parentheses. Pin 62 connects to the data write pin of the uC and the write-enable pin of the SRAM. Pin 69 connects to a status input pin of the PC parallel port and the PS/2 data line. Pin 68 connects to the PS/2 clock line.
68	P3.4(T0)_PS/2_CLK	
62	P3.6(WRB)_WEB	
27	P3.7(RDB)	
41	P0.0(AD0)_D0	These pins connect to Port 0 of the uC which is also a multiplexed address/data port. These pins also connect to the data pins of the SRAM.
40	P0.1(AD1)_D1	
39	P0.2(AD2)_D2	
38	P0.3(AD3)_D3	
35	P0.4(AD4)_D4	
81	P0.5(AD5)_D5	
80	P0.6(AD6)_D6	
10	P0.7(AD7)_D7	
59	P2.0(A8)_A8	These pins connect to Port 2 of the uC which also outputs the upper address byte. These pins also connect to the upper address bits of the SRAM. Pins 28 and 16 are connected to the 128 KB SRAM address pins only on the XS40+ Board. Pins 28 and 16 do not connect to the 32 KB SRAM on the XS40 Board.
57	P2.0(A9)_A9	
51	P2.0(A10)_A10	
56	P2.0(A11)_A11	
50	P2.0(A12)_A12	
58	P2.0(A13)_A13	
60	P2.0(A14)_A14	
28	P2.0(A15)_A15	
16	A16	
3	A0	These pins drive the 8 lower address bits of the SRAM.
4	A1	
5	A2	
78	A3	
79	A4	
82	A5	
83	A6	
84	A7	
61	OEB	Pin that drives the SRAM output enable
65	CEB	Pin that drives the SRAM chip enable
75	PC_S7	Pin that drives a status input pin of the PC parallel port

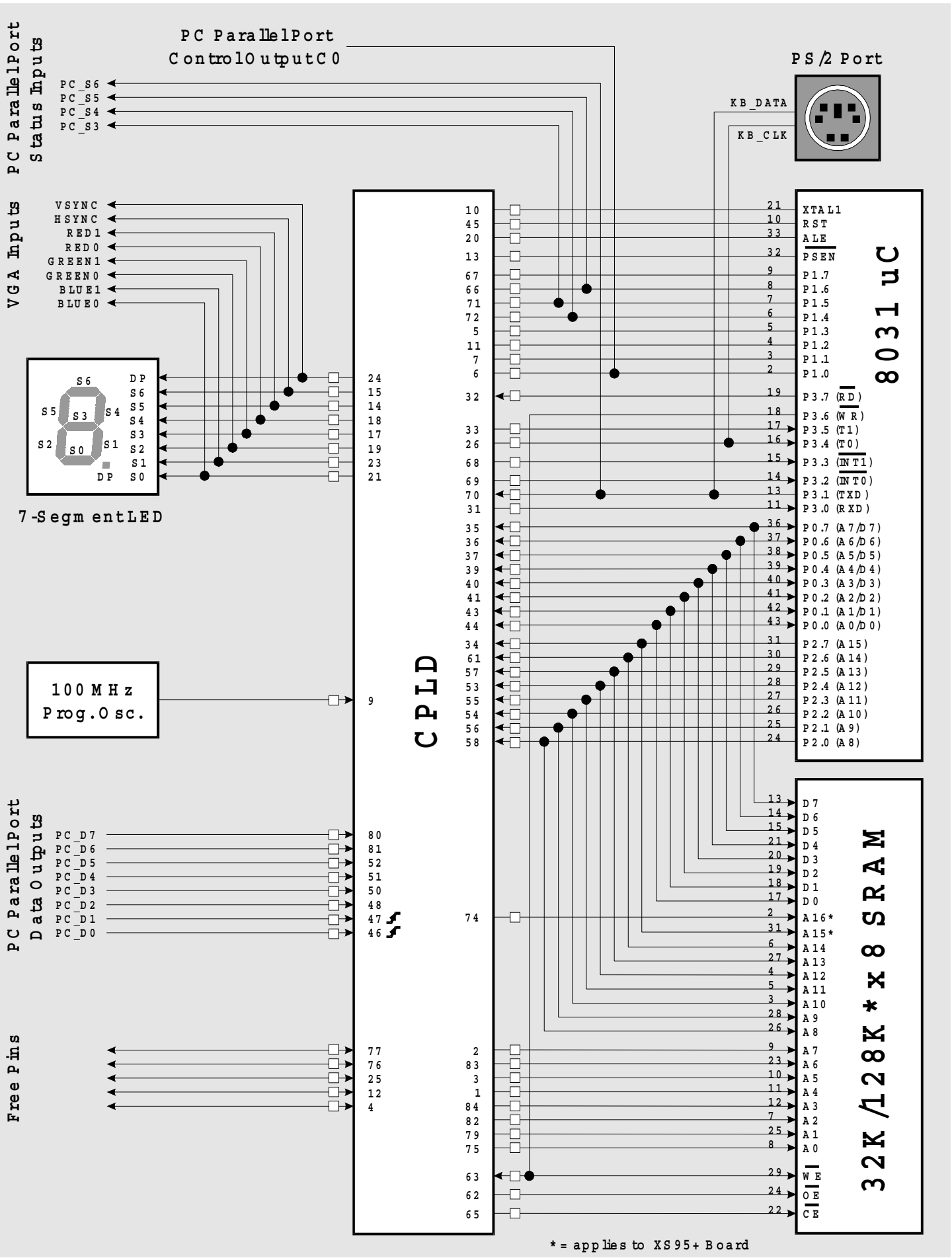

PC Parallel Port Status Inputs
PC_S7
PC_S6
PC_S5
PC_S4
PC_S3
PS/2 Port
KB_DATA
KB_CLK
VGA Inputs
VSYNC
HSYNC
RED1
RED0
GREEN1
GREEN0
BLUE1
BLUE0
S6
S5
S4
S3
S2
S1
S0
7-Segment LED
100 MHz Prog. Osc.
13
FPGA
37
36
29
14
67
66
70
77
6
9
8
7
27
68
75
69
10
80
81
35
38
39
40
41
28
60
58
50
56
51
57
59
84
83
82
79
78
5
4
3
62
61
65
8031 uC
21 XTAL1
10 RST
33 ALE
32 PSEN
9 P1.7
8 P1.6
7 P1.5
6 P1.4
5 P1.3
4 P1.2
3 P1.1
2 P1.0
19 P3.7 (RD)
18 P3.6 (WR)
17 P3.5 (T1)
16 P3.4 (T0)
15 P3.3 (INT1)
14 P3.2 (INT0)
13 P3.1 (TXD)
11 P3.0 (RXD)
36 P0.7 (A7/D7)
37 P0.6 (A6/D6)
38 P0.5 (A5/D5)
39 P0.4 (A4/D4)
40 P0.3 (A3/D3)
41 P0.2 (A2/D2)
42 P0.1 (A1/D1)
43 P0.0 (A0/D0)
31 P2.7 (A15)
30 P2.6 (A14)
29 P2.5 (A13)
28 P2.4 (A12)
27 P2.3 (A11)
26 P2.2 (A10)
25 P2.1 (A9)
24 P2.0 (A8)
32K/128K** x 8 SRAM
13 D7
14 D6
15 D5
21 D4
20 D3
19 D2
18 D1
17 D0
2 A16**
31 A15**
6 A14
27 A13
4 A12
5 A11
3 A10
28 A9
26 A8
9 A7
23 A6
10 A5
11 A4
12 A3
7 A2
25 A1
8 A0
29 WE
24 OE
22 CE
PC Parallel Port Data Outputs
PC_D7*
PC_D6*
PC_D5
PC_D4
PC_D3
PC_D2
PC_D1
PC_D0
34*
32*
49
48
47
46
45
44
16
* = not connected on XSP Board
** = applies to XS40+ Board


U1
XC4005XL
U2
U3A
U3B
U3C
U3F
74LS14
U4
DS1075
U5
7805
U7
AT17C256
U8A 4.7K
U8B 4.7K
U8C 4.7K
U8D 4.7K
U9
LM317
U10
8031-PLCC
U11A 330
U11B 680
U11C 680
U11D 330
U6A 680
U6B 680
U6C 680
U6D 680
U12A 10K
U12B 10K
U12C 10K
U12D 10K
U12E 10K
U12F 10K
U12G 10K
U12H 10K
U13A 4.7K
U13B 4.7K
U13C 4.7K
U13D 4.7K
U14A 10K
U14B 10K
U15
128X8 SRAM
R1 110
R5 464
R8 1400
R9 1690
C1 22uF 10V
C2 22uF 10V
C3 0.1uf
C4 0.1uf
C5 0.1uf
C6 0.1uf
C7 0.1uf
C8 0.1uf
C9 0.1uf
C10 0.1uf
D1
J9
CENTER
SIDE
SWITCH
J10
J11
J12
J1-1 TMS from PC
J1-2 blue
J1-3 green
J1-7 red
J1-8 vsync
J1-9 hsync
J1-11 drive TDO to PC
J1-14 TCLK from PC
J1-16
J1-17 DIN input comes from PC
J2-5
J2-6
J2-7
J2-8
J2-10
J2-14 vsync
J2-13 hsync
J2-1 red
J2-2 green
J2-3 blue
J3-1
J3-31
J3-33
J3-42
J3-43
J3-63
J3-74
J3-76
J3-64
J3-2
J3-52
J3-54
J3-11
J3-12
J3-21
J3-22
J5-1
J5-2
J5-3
J5-4
J5-5
J5-6
J4
J6
J7
J8
+5V
+3.3V
GND
XCBUS[01:84]
XCBUS30
XCBUS32
XCBUS34
XCBUS69
XCBUS68
XCBUS75
XCBUS73
XCBUS71
XCBUS55
XCBUS17
XCBUS49
XCBUS48
XCBUS47
XCBUS46
XCBUS45
XCBUS44
XCBUS13
XCBUS19
XCBUS23
XCBUS26
XCBUS25
XCBUS24
XCBUS22
XCBUS18
XCBUS41
XCBUS40
XCBUS39
XCBUS38
XCBUS35
XCBUS10
XCBUS80
XCBUS81
XCBUS67
XCBUS66
XCBUS77
XCBUS70
XCBUS36
XCBUS69
XCBUS68
XCBUS62
XCBUS27
XCBUS37
XCBUS28
XCBUS14
XCBUS29
XCBUS60
XCBUS58
XCBUS56
XCBUS51
XCBUS57
XCBUS59
XCBUS07
XCBUS08
XCBUS09
XCBUS06
XCBUS84
XCBUS83
XCBUS04
XCBUS50
XCBUS03
XCBUS78
XCBUS79
XCBUS82
XCBUS65
XCBUS61
XCBUS62
XCBUS16
DS1075
OSCIN_I/O
XTAL OUT/O
OE
PDN/SELX
8031-PLCC
P00
P01
P02
P03
P04
P05
P06
P07
P10
P11
P12
P13
P14
P15
P16
P17
P20
P21
P22
P23
P24
P25
P26
P27
P30
P31
P32
P33
P34
P35
P36
P37
RST
EA
ALE
PSEN
XTAL1
XTAL2
I/O,PGCK4
O,TDO
CCLK
DOUT
I/O,SGCK4
I/O,DIN
I/O,PGCK3
PROGRAM
DONE
I/O,SGCK3
I/O,SGCK1
I/O,PGCK1
I/O,TDI
I/O,TCK
I/O,TMS
I/O,SGCK2
I/O,M1
I/O,M0
I/O,M2
I/O,PGCK2
I/O,DOUT
I/O,LDC
I/O,INIT
DIN input comes from PC

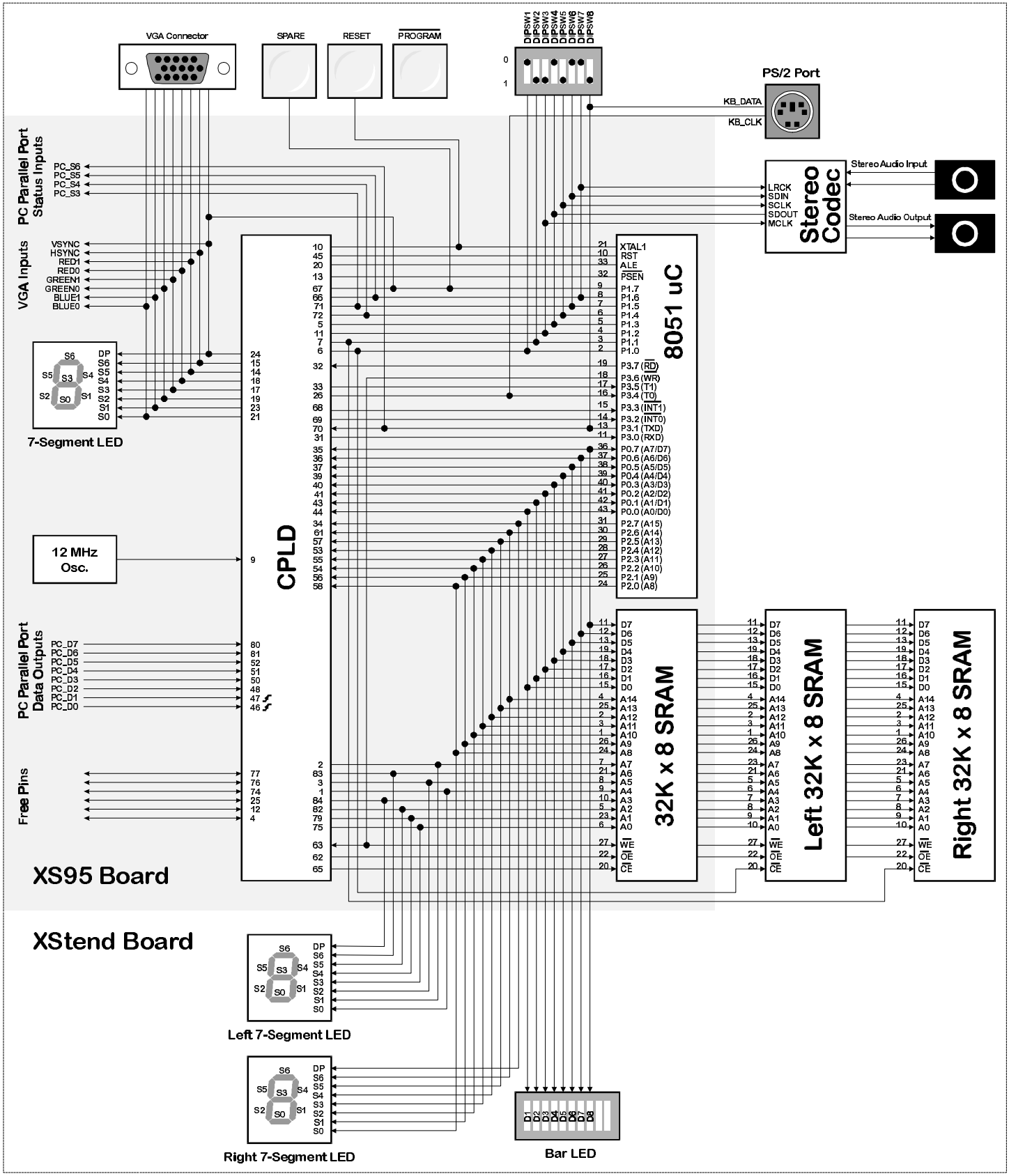
XS40 Pin (J1,J3,J18)	Power/ GND	DIP Switch	Push-buttons	LEDs	VGA Interface	PS/2 Interface	RAMs	Stereo Codec	8051 uC	PC Parallel Port	Oscillator	Function
2	+5V											+5V power source
3				LSB0			A0					Left LED segment; RAM address line
4				LSB1			A1					Left LED segment; RAM address line
5				LSB2			A2					Left LED segment; RAM address line
6		DIPSW4						SDOUT	P1.3			DIP switch; codec serial data output; uC I/O
7		DIPSW1					LCEB		P1.0			DIP switch; left RAM chip-enable, uC I/O port
8		DIPSW2					RCEB		P1.1			DIP switch; right RAM chip-enable, uC I/O port
9		DIPSW3						MCLK	P1.2			DIP switch; codec master clock; uC I/O port
10				DB8			D7		P0.7			LED; RAM data line; uC muxed address/data line
13											CLK	XS Board oscillator
14									PSENB			uC program store-enable
15												JTAG TDI; DIN
16												JTAG TCK; CCLK
17												JTAG TMS
18				S5	RED1							XS Board LED segment; VGA color signal
19				S6	HSYNCB							XS Board LED segment; VGA horiz. sync.
20				S3	GREEN1							XS Board LED segment; VGA color signal
23				S4	RED0							XS Board LED segment; VGA color signal
24				S2	GREEN0							XS Board LED segment; VGA color signal
25				S0	BLUE0							XS Board LED segment; VGA color signal
26				S1	BLUE1							XS Board LED segment; VGA color signal
27									P3.7 (RD_)			uC read line
28				RDPB					P2.7			Right LED decimal-point; uC I/O port
29									ALEB			uC address-latch-enable
30												Serial EEPROM chip-enable
32										PC_D6		PC parallel port data output
34										PC_D7		PC parallel port data output
35				DB5			D4		P0.4			LED; RAM data line; uC muxed address/data line
36									RST			uC reset
37			RESETB						XTAL1			Pushbutton; uC clock
38				DB4			D3		P0.3			LED; RAM data line; uC muxed address/data line
39				DB3			D2		P0.2			LED; RAM data line; uC muxed address/data line
40				DB2			D1		P0.1			LED; RAM data line; uC muxed address/data line
41				DB1			D0		P0.0			LED; RAM data line; uC muxed address/data line
44								CCLK		PC_D0		Codec control line; PC parallel port data output
45								CDIN		PC_D1		Codec control line; PC parallel port data output
46								CSB		PC_D2		Codec control line; PC parallel port data output
47										PC_D3		PC parallel port data output
48										PC_D4		PC parallel port data output
49										PC_D5		PC parallel port data output
50				RSB4			A12		P2.4			Right LED segment; RAM address line; uC I/O port
51				RSB2			A10		P2.2			Right LED segment; RAM address line; uC I/O port
52	GND											Power supply ground
54	5.0V/3.3V											5V/3.3V power supply (4000E/4000XL)
55			PROGRAM									XS40 configuration control
56				RSB3			A11		P2.3			Right LED segment; RAM address line; uC I/O port
57				RSB1			A9		P2.1			Right LED segment; RAM address line; uC I/O port
58				RSB5			A13		P2.5			Right LED segment; RAM address line; uC I/O port
59				RSB0			A8		P2.0			Right LED segment; RAM address line; uC I/O port
60				RSB6			A14		P2.6			Right LED segment; RAM address line; uC I/O port
61							OEB					RAM output-enable
62							WEB		P3.6 (WR_)			RAM write-enable; uC I/O port
65							CEB					XS Board RAM chip-enable
66		DIPSW7						LRCK	P1.6	PC_S5		DIP switch; codec left-right channel switch; uC I/O port; PC parallel port status in
67			SPAREB		VSYNCB				P1.7			Pushbutton; VGA vert. sync.; uC I/O port
68						KB_CLK			P3.4 (T0)			PS/2 keyboard clock; uC I/O port
69		DIPSW8				KB_DATA			P3.1 (TXD)	PC_S6		DIP switch; PS/2 keyboard serial data; uC I/O port; PC parallel port status input
70		DIPSW6						SDIN	P1.5	PC_S3		DIP switch; codec serial input data; uC I/O port; PC parallel port status input
71												JTAG TDI; DIN
72												JTAG TDO; DOUT
73												JTAG TCK; CCLK
75										PC_S7		JTAG TDO; DOUT; PC parallel port status input
77		DIPSW5						SCLK	P1.4	PC_S4		DIP switch; codec serial I/O clock; uC I/O port; PC parallel port status input
78				LSB3			A3					Left LED segment; RAM address line
79				LSB4			A4					Left LED segment; RAM address line
80				DB7			D6		P0.6			LED; RAM data line; uC muxed address/data line
81				DB6			D5		P0.5			LED; RAM data line; uC muxed address/data line
82				LSB5			A5					Left LED segment; RAM address line
83				LSB6			A6					Left LED segment; RAM address line
84				LDPB			A7					Left LED decimal-point; RAM address line

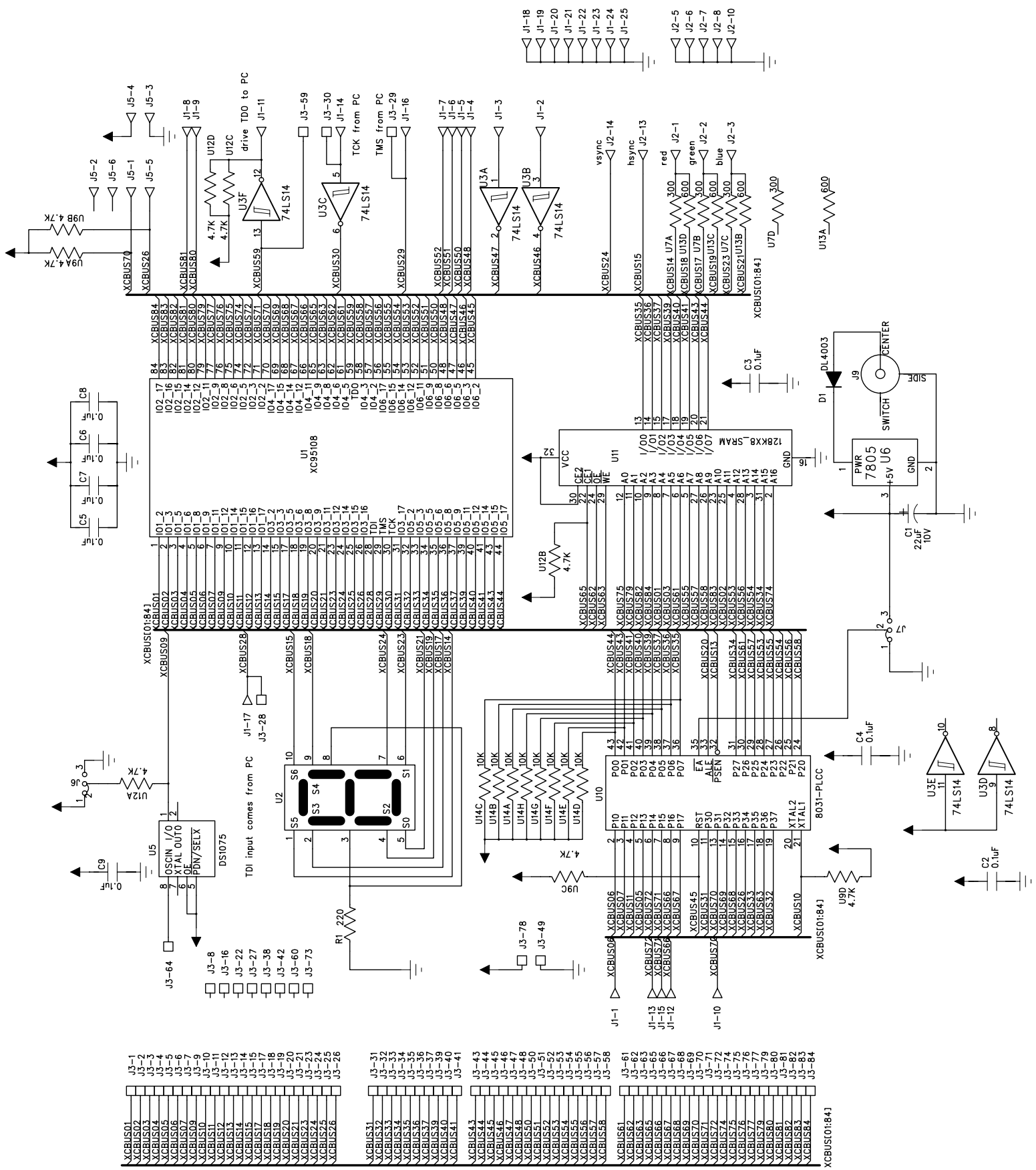

VGA Connector
SPARE
RESET
PROGRAM
DIPSW1
DIPSW2
DIPSW3
DIPSW4
DIPSW5
DIPSW6
DIPSW7
DIPSW8
PS/2 Port
KB_DATA
KB_CLK
PC Parallel Port Status Inputs
PC_S7
PC_S6
PC_S5
PC_S4
PC_S3
VGA Inputs
VSYNC
HSYNC
RED1
RED0
GREEN1
GREEN0
BLUE1
BLUE0
Stereo Codec
LRCK
SDIN
SCLK
SDOUT
MCLK
Stereo Audio Input
Stereo Audio Output
7-Segment LED
FPGA
8051 uC
12 MHz Osc.
PC Parallel Port Data Outputs
PC_D7
PC_D6
PC_D5
PC_D4
PC_D3
PC_D2
PC_D1
PC_D0
32K x 8 SRAM
Left 32K x 8 SRAM
Right 32K x 8 SRAM
XS40 Board
XStend Board
Left 7-Segment LED
Right 7-Segment LED
Bar LED

XS95 Pin	Connects to...	Description
21	S0.BLUE0	These pins drive the individual segments of the LED display (S0-S6 and DP). They also drive the color, horizontal, and vertical sync signals for a VGA monitor.
23	S1.BLUE1	
19	S2.GREEN0	
17	S3.GREEN1	
18	S4.RED0	
14	S5.RED1	
15	S6.HSYNCB	
24	DP.VSYNCB	
9	CLK	An input driven by the 100 MHz programmable oscillator.
46	PC_D0	These pins are driven by the data output pins of the PC parallel port. Clocking signals can only be reliably applied through pins 46 and 47 since these have additional hysterisis circuitry.
47	PC_D1	
48	PC_D2	
50	PC_D3	
51	PC_D4	
52	PC_D5	
81	PC_D6	
80	PC_D7	
10	XTAL1	Pin that drives the uC clock input
45	RST	Pin that drives the uC reset input
20	ALEB	Pin that monitors the uC address latch enable
13	PSENB	Pin that monitors the uC program store enable
6	P1.0, PC_C0	These pins connect to the pins of Port 1 of the uC. Some of the pins are also connected to the status input pins of the PC parallel port. The P1.0 port pin of the uC is also connected to the C0 control output from the parallel port.
7	P1.1	
11	P1.2	
5	P1.3	
72	P1.4,PC_S4	
71	P1.5,PC_S3	
66	P1.6,PC_S5	
67	P1.7	
31	P3.0(RXD)	These pins connect to the pins of Port 3 of the uC. The uC has specialized functions for each of the port pins indicated in parentheses. Pin 63 connects to the data write pin of the uC and the write-enable pin of the SRAM. Pins 26 and 70 connect to the clock and data lines of the PS/2 port. Pin 70 connects to a status input pin of the PC parallel port.
70	P3.1(TXD), PC_S6, KB_DATA	
69	P3.2(INTB0)	
68	P3.3(INTB1)	
26	P3.4(T0), KB_CLK	
33	P3.5(T1)	
63	P3.6(WRB), WEB	
32	P3.7(RDB)	
44	P0.0(AD0), D0	These pins connect to Port 0 of the uC which is also a multiplexed address/data port. These pins also connect to the data pins of the SRAM.
43	P0.1(AD1), D1	
41	P0.2(AD2), D2	
40	P0.3(AD3), D3	
39	P0.4(AD4), D4	
37	P0.5(AD5), D5	
36	P0.6(AD6), D6	
35	P0.7(AD7), D7	
58	P2.0(A8), A8	These pins connect to Port 2 of the uC which also outputs the upper address byte. These pins also connect to the upper address bits of the SRAM. Pins 34 and 74 are connected to the 128 KB SRAM address pins only on the XS95+ Board. Pins 34 and 74 do not connect to the 32 KB SRAM on the XS95 Board.
56	P2.0(A9), A9	
54	P2.0(A10), A10	
55	P2.0(A11), A11	
53	P2.0(A12), A12	
57	P2.0(A13), A13	
61	P2.0(A14), A14	
34	P2.0(A15),A15	
74	A16	
75	A0	These pins drive the 8 lower address bits of the SRAM.
79	A1	
82	A2	
84	A3	
1	A4	
3	A5	
83	A6	
2	A7	
62	OEB	Pin that drives the SRAM output enable.
65	CEB	Pin that drives the SRAM chip enable.
4	FREE0	These pins are not connected to other devices and can be used as general purpose I/O.
12	FREE1	
25	FREE2	
76	FREE3	
77	FREE4	


PC Parallel Port Status Inputs
PC_S6
PC_S5
PC_S4
PC_S3
PC Parallel Port Control Output C0
PS/2 Port
KB_DATA
KB_CLK
VGA Inputs
VSYNC
HSYNC
RED1
RED0
GREEN1
GREEN0
BLUE1
BLUE0
7-Segment LED
100 MHz Prog. Osc.
PC Parallel Port Data Outputs
PC_D7
PC_D6
PC_D5
PC_D4
PC_D3
PC_D2
PC_D1
PC_D0
Free Pins
CPLD
8031 uC
XTAL1
RST
ALE
PSEN
P1.7
P1.6
P1.5
P1.4
P1.3
P1.2
P1.1
P1.0
P3.7 (RD)
P3.6 (WR)
P3.5 (T1)
P3.4 (T0)
P3.3 (INT1)
P3.2 (INT0)
P3.1 (TXD)
P3.0 (RXD)
P0.7 (A7/D7)
P0.6 (A6/D6)
P0.5 (A5/D5)
P0.4 (A4/D4)
P0.3 (A3/D3)
P0.2 (A2/D2)
P0.1 (A1/D1)
P0.0 (A0/D0)
P2.7 (A15)
P2.6 (A14)
P2.5 (A13)
P2.4 (A12)
P2.3 (A11)
P2.2 (A10)
P2.1 (A9)
P2.0 (A8)
32K/128K*x8 SRAM
D7
D6
D5
D4
D3
D2
D1
D0
A16*
A15*
A14
A13
A12
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
WE
OE
CE
* = applies to XS95+ Board

XS95 Pins (J2)	Power/ GND	DIP Switch	Push-buttons	LEDs	VGA Interface	PS/2 Interface	RAMs	Stereo Codec	8051 Uc	PC Parallel Port	Oscillator	Function
1				LSB0			A4					Left LED segment; RAM address line
2				LSB1			A7					Left LED segment; RAM address line
3				LSB2			A5					Left LED segment; RAM address line
4												Uncommitted XS95 I/O pin
5		DIPSW4						SDOUT	P1.3			DIP switch; codec serial data output; uC I/O
6		DIPSW1					LCEB		P1.0			DIP switch; left RAM chip-enable, uC I/O port
7		DIPSW2					RCEB		P1.1			DIP switch; right RAM chip-enable, uC I/O port
9											CLK	XS Board oscillator
10			RESETB						XTAL1			Pushbutton; uC clock
11		DIPSW3						MCLK	P1.2			DIP switch; codec master clock; uC I/O port
12												Uncommitted XS95 I/O pin
13									PSENB			uC program store-enable
14				S5	RED1							XS Board LED segment; VGA color signal
15				S6	HSYNCB							XS Board LED segment; VGA horiz. sync.
17				S3	GREEN1							XS Board LED segment; VGA color signal
18				S4	RED0							XS Board LED segment; VGA color signal
19				S2	GREEN0							XS Board LED segment; VGA color signal
20									ALEB			uC address-latch-enable
21				S0	BLUE0							XS Board LED segment; VGA color signal
23				S1	BLUE1							XS Board LED segment; VGA color signal
25												Uncommitted XS95 I/O pin
26						KB_CLK			P3.4 (T0)			PS/2 keyboard clock; uC I/O port
28												JTAG TDI; DIN
29												JTAG TMS
30												JTAG TCK; CCLK
31									P3.0 (RXD)			uC I/O port
32									P3.7 (RD_)			uC I/O port
33									P3.5 (T1)			uC I/O port
34				RDPB					P2.7			Right LED decimal-point; RAM address line; uC I/O port
35				DB8			D7		P0.7			LED; RAM data line; uC muxed address/data line
36				DB7			D6		P0.6			LED; RAM data line; uC muxed address/data line
37				DB6			D5		P0.5			LED; RAM data line; uC muxed address/data line
39				DB5			D4		P0.4			LED; RAM data line; uC muxed address/data line
40				DB4			D3		P0.3			LED; RAM data line; uC muxed address/data line
41				DB3			D2		P0.2			LED; RAM data line; uC muxed address/data line
43				DB2			D1		P0.1			LED; RAM data line; uC muxed address/data line
44				DB1			D0		P0.0			LED; RAM data line; uC muxed address/data line
45									RST			uC reset
46								CCLK		PC_D0		Codec control line; PC parallel port data output
47								CDIN		PC_D1		Codec control line; PC parallel port data output
48								CSB		PC_D2		Codec control line; PC parallel port data output
49	GND											Power supply ground
50										PC_D3		PC parallel port data output
51										PC_D4		PC parallel port data output
52										PC_D5		PC parallel port data output
53				RSB4			A12		P2.4			Right LED segment; RAM address line; uC I/O port
54				RSB2			A10		P2.2			Right LED segment; RAM address line; uC I/O port
55				RSB3			A11		P2.3			Right LED segment; RAM address line; uC I/O port
56				RSB1			A9		P2.1			Right LED segment; RAM address line; uC I/O port
57				RSB5			A13		P2.5			Right LED segment; RAM address line; uC I/O port
58				RSB0			A8		P2.0			Right LED segment; RAM address line; uC I/O port
59												JTAG TDO; DOUT
61				RSB6			A14		P2.6			Right LED segment; RAM address line; uC I/O port
62							OEB					RAM output-enable
63							WEB		P3.6 (WR_)			RAM write-enable; uC I/O port
65							CEB					XS Board RAM chip-enable
66		DIPSW7						LRCK	P1.6	PC_S5		DIP switch; codec left-right channel select; uC I/O port; PC parallel port status in
68									P3.3 (INT1_)			uC I/O port
69									P3.2 (INT0_)			uC I/O port
70		DIPSW8				KB_DATA			P3.1 (TXD)	PC_S6		DIP switch; PS/2 keyboard serial data; uC I/O port; PC parallel port status input
71		DIPSW6						SDIN	P1.5	PC_S3		DIP switch; codec serial input data; uC I/O port; PC parallel port status input
72		DIPSW5						SCLK	P1.4	PC_S4		DIP switch; codec serial clock; uC I/O port; PC parallel port status input
74												Uncommitted XS95 I/O pin
75				LSB3			A0					Left LED segment; RAM address line
76												Uncommitted XS95 I/O pin
77												Uncommitted XS95 I/O pin
78	+5V											+5V power source
79				LSB4			A1					Left LED segment; RAM address line
80										PC_D7		PC parallel port data output
81										PC_D6		PC parallel port data output
82				LSB5			A2					Left LED segment; RAM address line
83				LSB6			A6					Left LED segment; RAM address line
84				LDPB			A3					Left LED decimal-point; RAM address line
24,67			SPAREB	DP	VSYNCB				P1.7			Pushbutton; XS Board LED decimal-point; VGA horiz. sync.; uC I/O port

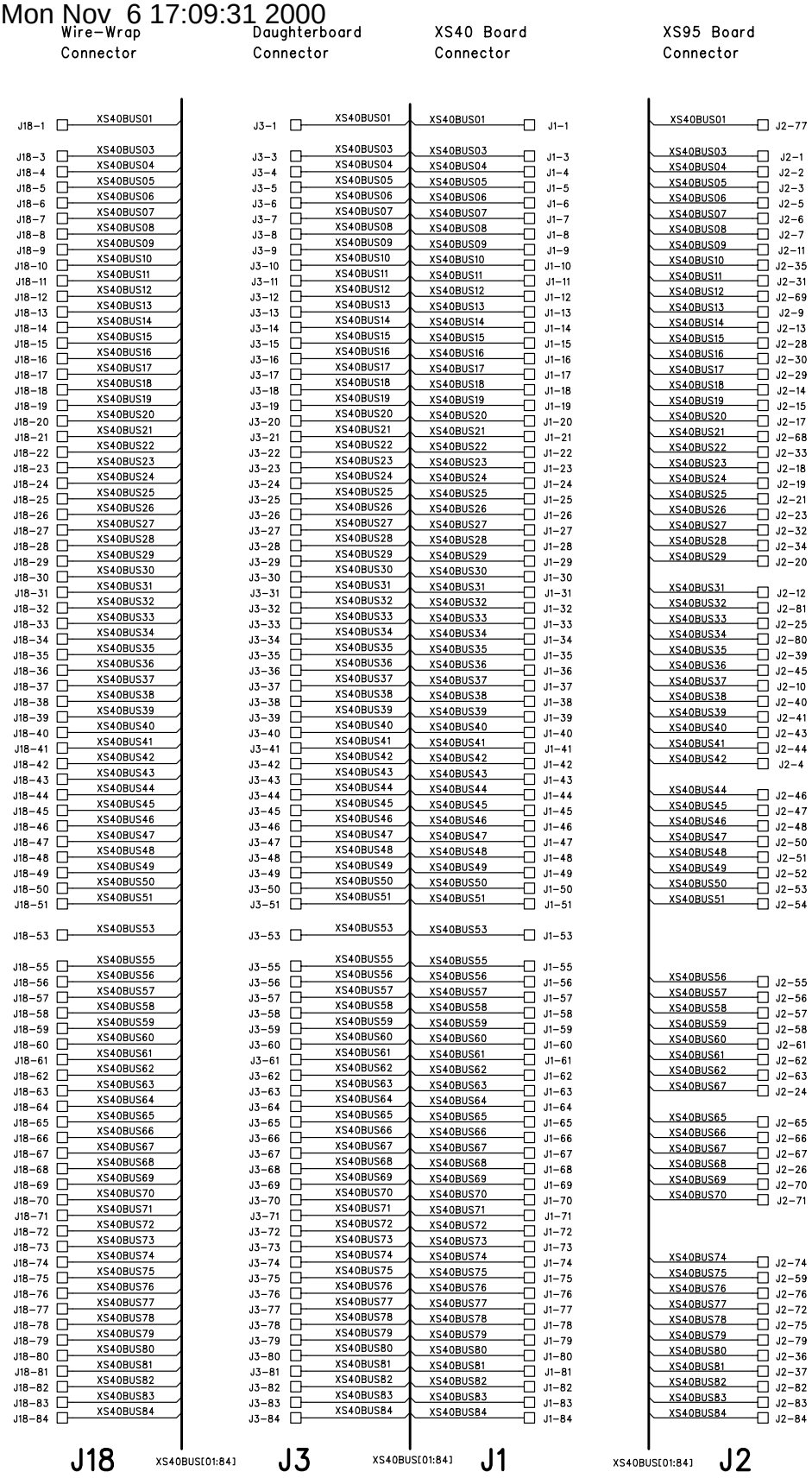

VGA Connector
SPARE
RESET
PROGRAM
DIPSW1
DIPSW2
DIPSW3
DIPSW4
DIPSW5
DIPSW6
DIPSW7
DIPSW8
PS/2 Port
KB_DATA
KB_CLK
PC Parallel Port Status Inputs
PC_S6
PC_S5
PC_S4
PC_S3
VGA Inputs
VSYNC
HSYNC
RED1
RED0
GREEN1
GREEN0
BLUE1
BLUE0
Stereo Codec
LRCK
SDIN
SCLK
SDOUT
MCLK
Stereo Audio Input
Stereo Audio Output
7-Segment LED
CPLD
8051 uC
12 MHz Osc.
PC Parallel Port Data Outputs
PC_D7
PC_D6
PC_D5
PC_D4
PC_D3
PC_D2
PC_D1
PC_D0
Free Pins
32K x 8 SRAM
Left 32K x 8 SRAM
Right 32K x 8 SRAM
XS95 Board
XStend Board
Left 7-Segment LED
Right 7-Segment LED
Bar LED


U1
XC95108
U11
128KX8_SRAM
8031-PLCC
U10
U2
DS1075
U5
U7A
U7B
U7C
U7D
U13A
U13B
U13C
U13D
U3A
U3B
U3C
U3D
U3E
U3F
U12A
U12B
U12C
U12D
U14A
U14B
U14C
U14D
U14E
U14F
U14G
U14H
U9A 4.7K
U9B 4.7K
U9C
U9D
R1 220
C1 22uF 10V
C2 0.1uF
C3 0.1uF
C4 0.1uF
C5 0.1uF
C6 0.1uF
C7 0.1uF
C8 0.1uF
C9 0.1uF
D1
DL4003
J9
CENTER
SIDE
SWITCH
PWR 7805 U6
+5V
GND
VCC
TDI input comes from PC
drive TDO to PC
TCK from PC
TMS from PC
vsync
hsync
red
green
blue
XCBUS[01:84]

Appendix

A

XStend Schematics


Wire-Wrap Connector
Daughterboard Connector
XS40 Board Connector
XS95 Board Connector
J18
J3
J1
J2
XS40BUS[01:84]
XS40BUS01
XS40BUS03
XS40BUS04
XS40BUS05
XS40BUS06
XS40BUS07
XS40BUS08
XS40BUS09
XS40BUS10
XS40BUS11
XS40BUS12
XS40BUS13
XS40BUS14
XS40BUS15
XS40BUS16
XS40BUS17
XS40BUS18
XS40BUS19
XS40BUS20
XS40BUS21
XS40BUS22
XS40BUS23
XS40BUS24
XS40BUS25
XS40BUS26
XS40BUS27
XS40BUS28
XS40BUS29
XS40BUS30
XS40BUS31
XS40BUS32
XS40BUS33
XS40BUS34
XS40BUS35
XS40BUS36
XS40BUS37
XS40BUS38
XS40BUS39
XS40BUS40
XS40BUS41
XS40BUS42
XS40BUS43
XS40BUS44
XS40BUS45
XS40BUS46
XS40BUS47
XS40BUS48
XS40BUS49
XS40BUS50
XS40BUS51
XS40BUS53
XS40BUS55
XS40BUS56
XS40BUS57
XS40BUS58
XS40BUS59
XS40BUS60
XS40BUS61
XS40BUS62
XS40BUS63
XS40BUS64
XS40BUS65
XS40BUS66
XS40BUS67
XS40BUS68
XS40BUS69
XS40BUS70
XS40BUS71
XS40BUS72
XS40BUS73
XS40BUS74
XS40BUS75
XS40BUS76
XS40BUS77
XS40BUS78
XS40BUS79
XS40BUS80
XS40BUS81
XS40BUS82
XS40BUS83
XS40BUS84
XS40BUS67
XS40BUS69
XS40BUS70
XS40BUS74
XS40BUS75
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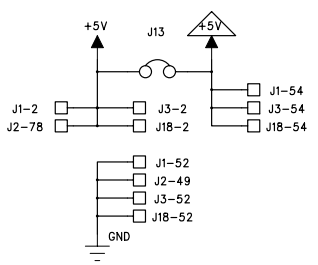
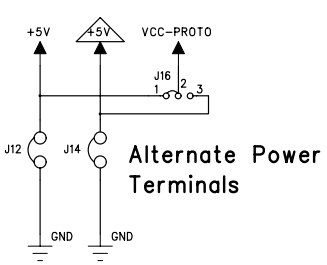
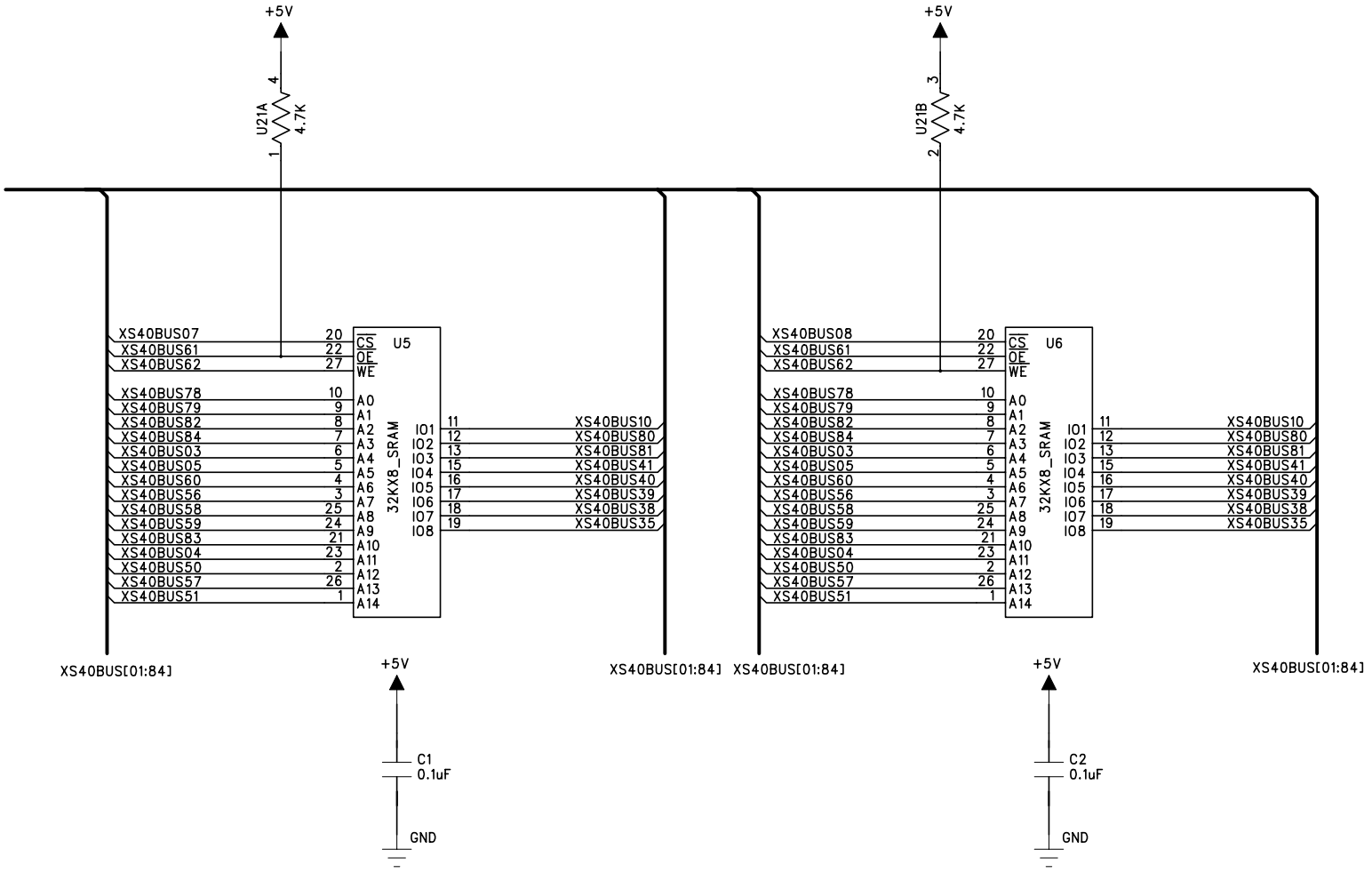
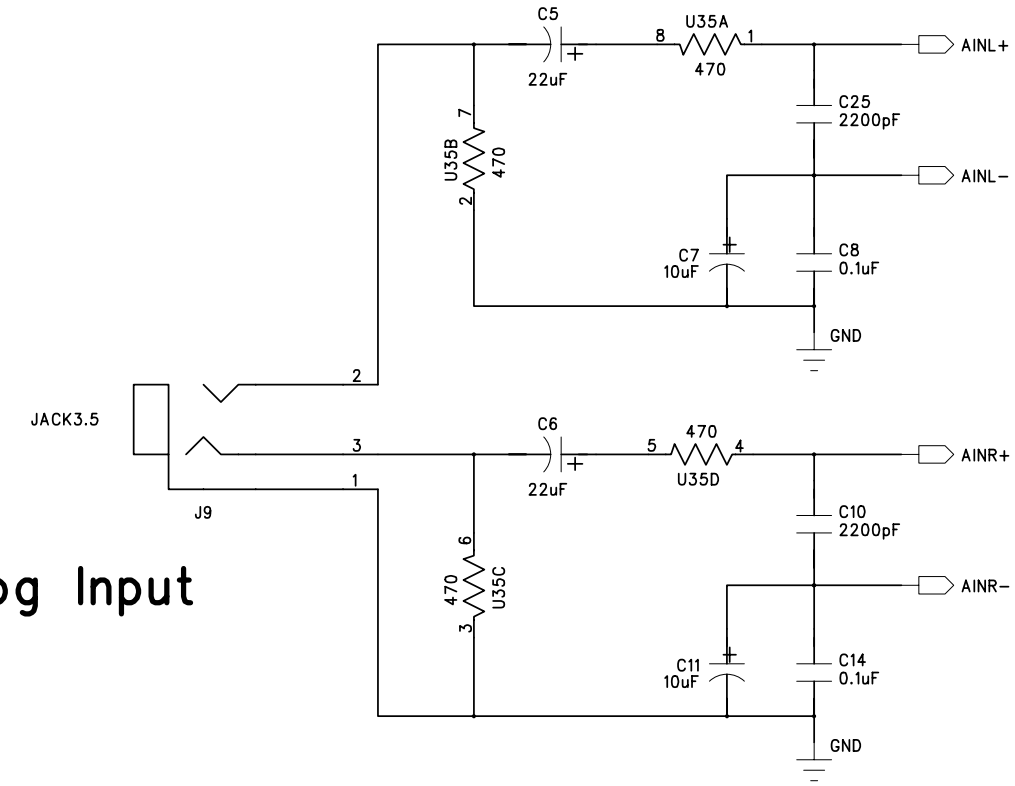
XS40BUS80
XS40BUS81
XS40BUS82
XS40BUS83
XS40BUS84

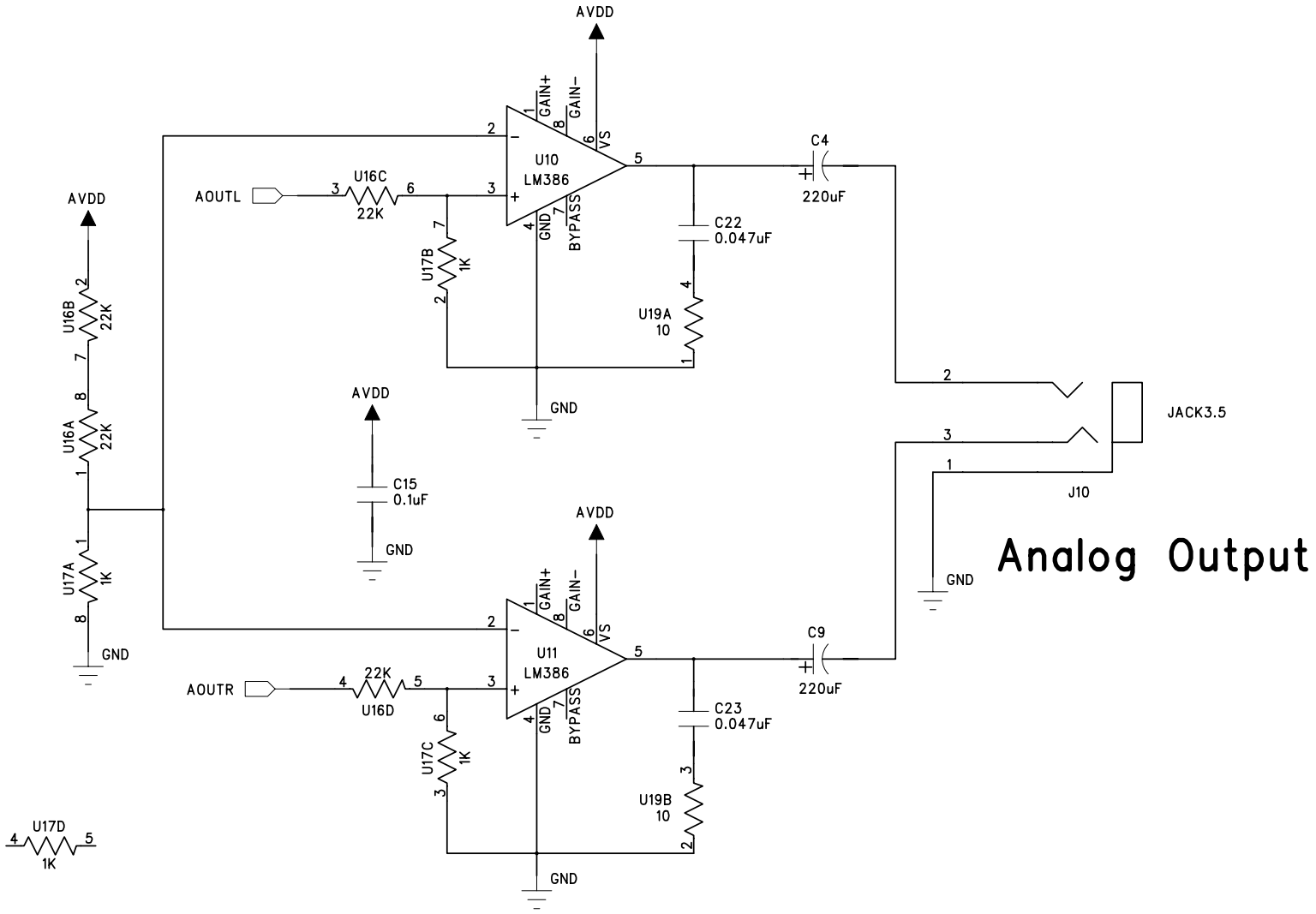

+5V
J13
+5V
J1-54
J3-54
J18-54
J1-2
J2-78
J3-2
J18-2
J1-52
J2-49
J3-52
J18-52
GND


+5V
+5V
VCC-PROTO
J16
1
2
3
J12
J14
Alternate Power Terminals
GND
GND

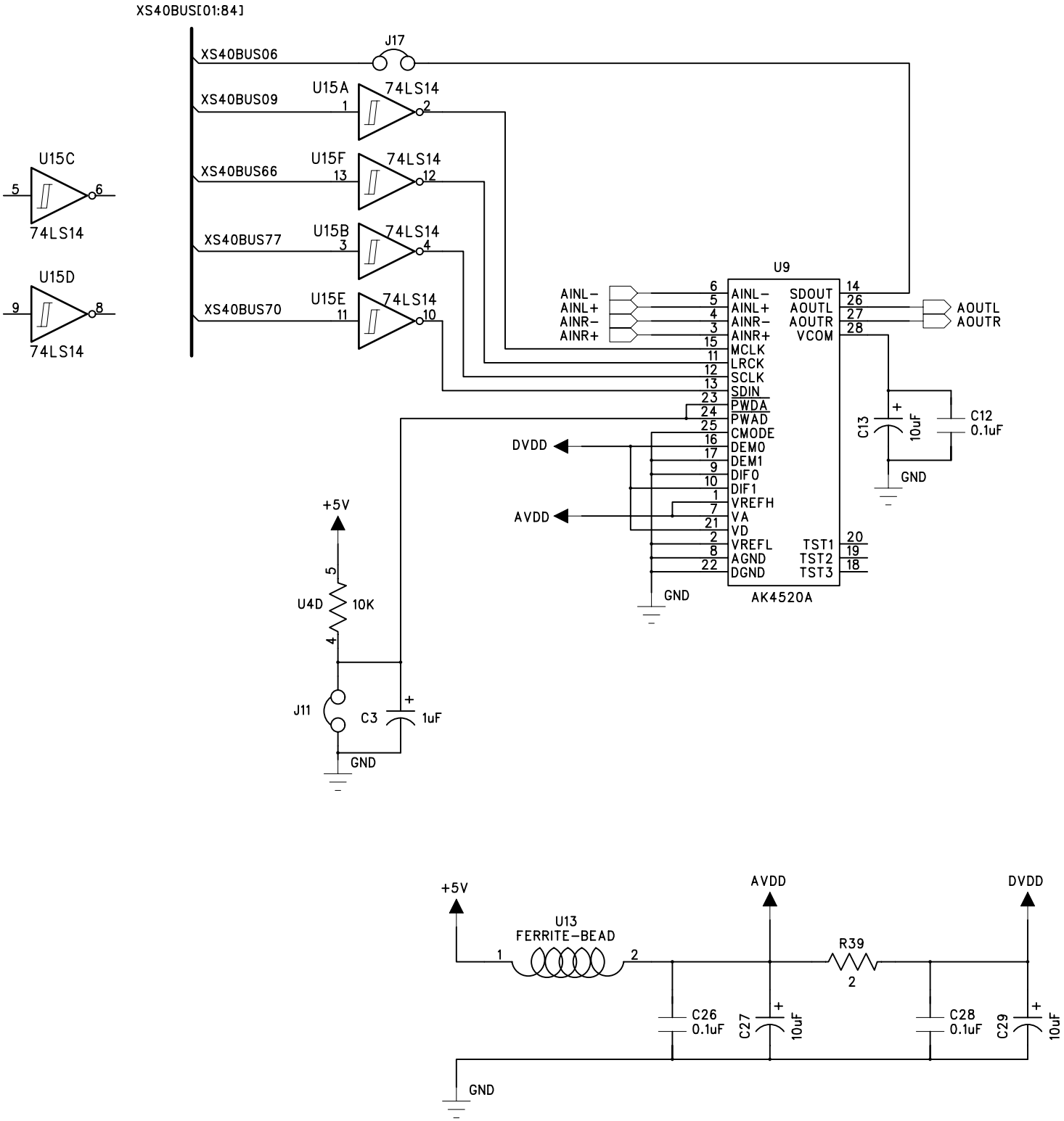

+5V
U21A
4.7K
+5V
U21B
4.7K
U5
U6
32KX8_SRAM
XS40BUS07
XS40BUS61
XS40BUS62
XS40BUS78
XS40BUS79
XS40BUS82
XS40BUS84
XS40BUS03
XS40BUS05
XS40BUS60
XS40BUS56
XS40BUS58
XS40BUS59
XS40BUS83
XS40BUS04
XS40BUS50
XS40BUS57
XS40BUS51
XS40BUS08
XS40BUS10
XS40BUS80
XS40BUS81
XS40BUS41
XS40BUS40
XS40BUS39
XS40BUS38
XS40BUS35
XS40BUS[01:84]
C1
C2
0.1uF
GND

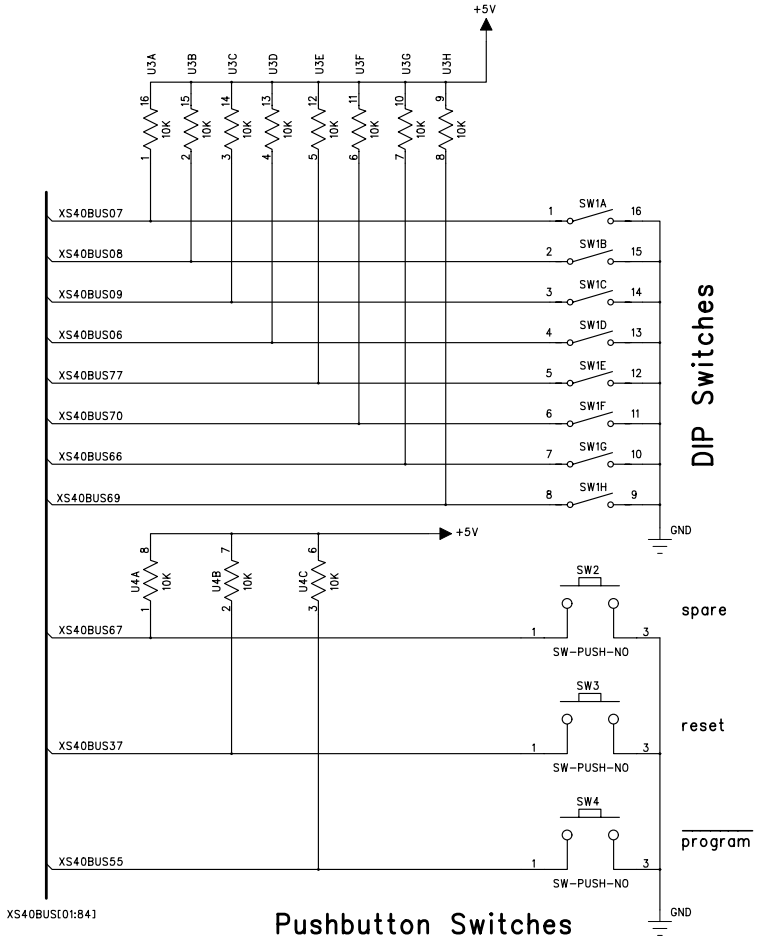


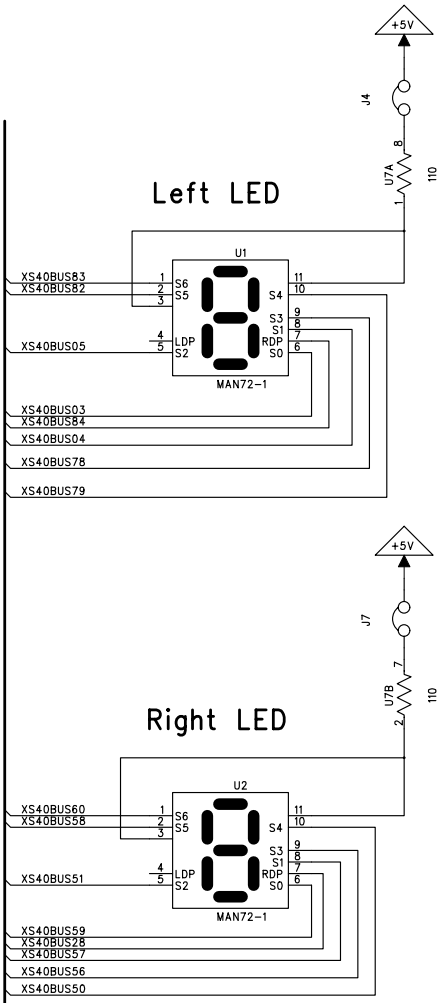
Analog Input

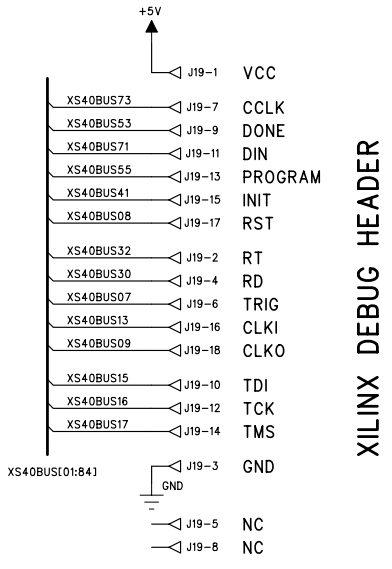


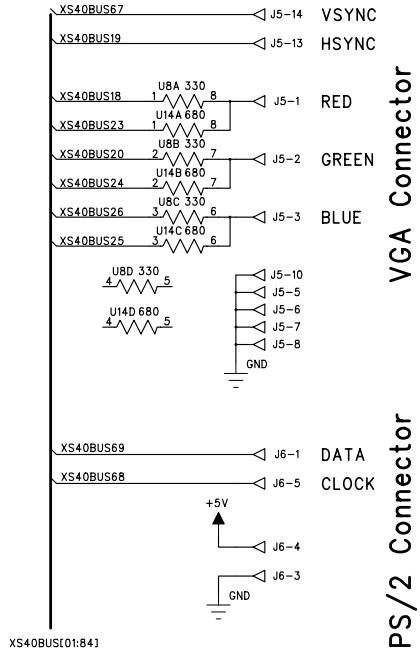
Analog Output

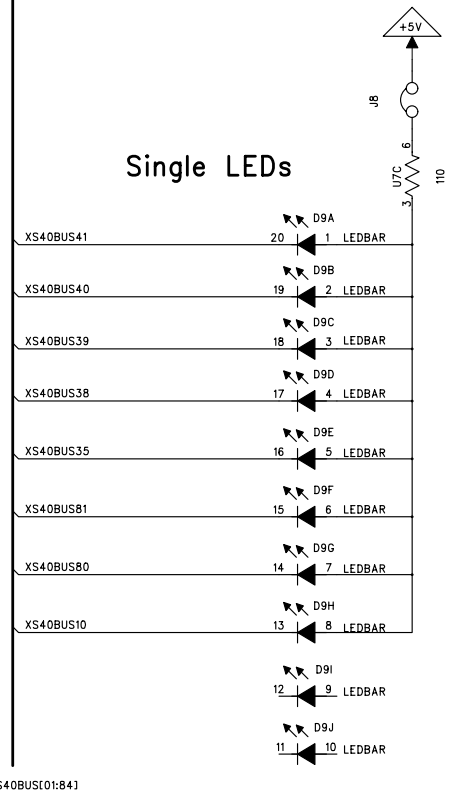

XS40BUS[01:84]
XS40BUS06
XS40BUS09
XS40BUS66
XS40BUS77
XS40BUS70
J17
U15A
U15B
U15C
U15D
U15E
U15F
74LS14
U9
AINL-
AINL+
AINR-
AINR+
MCLK
LRCK
SCLK
SDIN
PWDA
PWAD
CMODE
DEM0
DEM1
DIF0
DIF1
VREFH
VA
VD
VREFL
AGND
DGND
SDOUT
AOUTL
AOUTR
VCOM
TST1
TST2
TST3
AK4520A
AOUTL
AOUTR
C12
0.1uF
C13
10uF
DVDD
AVDD
GND
+5V
U4D
10K
J11
C3
1uF
U13
FERRITE-BEAD
R39
C26
0.1uF
C27
10uF
C28
0.1uF
C29
10uF


+5V
U3A 10K
U3B 10K
U3C 10K
U3D 10K
U3E 10K
U3F 10K
U3G 10K
U3H 10K
XS40BUS07
XS40BUS08
XS40BUS09
XS40BUS06
XS40BUS77
XS40BUS70
XS40BUS66
XS40BUS69
SW1A
SW1B
SW1C
SW1D
SW1E
SW1F
SW1G
SW1H
DIP Switches
GND
U4A 10K
U4B 10K
U4C 10K
SW2
spare
XS40BUS67
SW-PUSH-NO
SW3
reset
XS40BUS37
SW4
program
XS40BUS55
XS40BUS[01:84]
Pushbutton Switches


+5V
J4
U7A 110
Left LED
U1
XS40BUS83
XS40BUS82
XS40BUS05
S6
S5
S4
S3
S1
RDP
S0
LDP
S2
MAN72-1
XS40BUS03
XS40BUS84
XS40BUS04
XS40BUS78
XS40BUS79
J7
U7B 110
Right LED
U2
XS40BUS60
XS40BUS58
XS40BUS51
XS40BUS59
XS40BUS28
XS40BUS57
XS40BUS56
XS40BUS50
U7D 110


+5V
J19-1 VCC
XS40BUS73 J19-7 CCLK
XS40BUS53 J19-9 DONE
XS40BUS71 J19-11 DIN
XS40BUS55 J19-13 PROGRAM
XS40BUS41 J19-15 INIT
XS40BUS08 J19-17 RST
XS40BUS32 J19-2 RT
XS40BUS30 J19-4 RD
XS40BUS07 J19-6 TRIG
XS40BUS13 J19-16 CLKI
XS40BUS09 J19-18 CLKO
XS40BUS15 J19-10 TDI
XS40BUS16 J19-12 TCK
XS40BUS17 J19-14 TMS
XS40BUS[01:84]
J19-3 GND
GND
J19-5 NC
J19-8 NC
XILINX DEBUG HEADER


XS40BUS67
J5-14 VSYNC
XS40BUS19
J5-13 HSYNC
XS40BUS18
U8A 330
J5-1 RED
XS40BUS23
U14A 680
XS40BUS20
U8B 330
J5-2 GREEN
XS40BUS24
U14B 680
XS40BUS26
U8C 330
J5-3 BLUE
XS40BUS25
U14C 680
U8D 330
U14D 680
J5-10
J5-5
J5-6
J5-7
J5-8
GND
VGA Connector
XS40BUS69
J6-1 DATA
XS40BUS68
J6-5 CLOCK
+5V
J6-4
J6-3
GND
XS40BUS[01:84]
PS/2 Connector


+5V
J8
U7C 110
Single LEDs
XS40BUS41
D9A
LEDBAR
XS40BUS40
D9B
XS40BUS39
D9C
XS40BUS38
D9D
XS40BUS35
D9E
XS40BUS81
D9F
XS40BUS80
D9G
XS40BUS10
D9H
D9I
D9J
XS40BUS[01:84]

A

XStend + XSA Pin Connections

The following table lists the connections between the XStend Board components and the components of the XSA Board. The columns of the table are arranged as follows:

Column 1 lists the pin number for the Spartan-II FPGA on the XSA Board. It is left blank if there is no connection to the FPGA for this function. Pins marked with * are useable as general-purpose I/O through the prototyping header; pins marked with ** can be used as general-purpose I/O only if the CPLD interface is reprogrammed so it doesn't drive this pin; pins with no marking cannot be used as general-purpose I/O at all.

Column 2 lists the pin number for the XC9572XL CPLD on the XSA Board. It is left blank if there is no connection to the CPLD for this function.

Column 3 lists the functions of other devices on the XSA Board that are connected to the associated FPGA and/or CPLD pin.

Column 4 lists the pin of the XSA prototyping header that is connected to the associated FPGA and/or CPLD pin.

Columns 5–7 list the pins of devices on the XStend Board that will connect to the FPGA and/or CPLD when the XSA Board is inserted into an XStend Board.

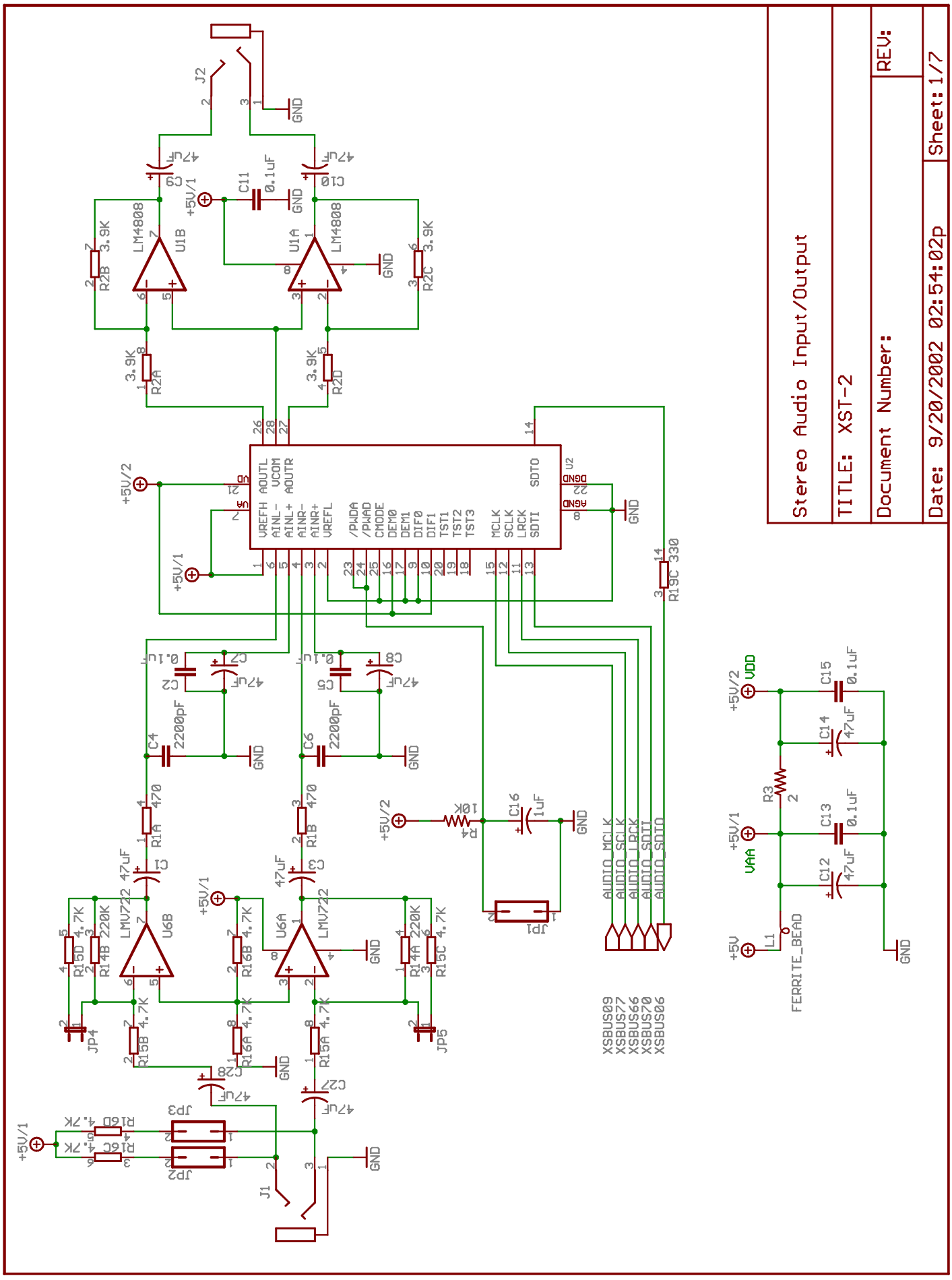
FPGA	CPLD	XSA Function	Proto. Pin	XStend V2.0 Functions		
1		+3.3V	54	+3.3V		
2	13	SPARTAN-TCK	16			
3		SDRAM-A7				
4		SDRAM-A1				
5		SDRAM-A6				
6		SDRAM-A2				
7		SDRAM-A5				
8		GND	52	GND		
9		+2.5V	22			
10		SDRAM-A3				
11		SDRAM-A4				
12*		VGA-RED0	27			
13*		VGA-RED1	28			
15*		SPARTAN-GCK3	31			
18*		SPARTAN-GCK2	1			
19*		VGA-GREEN0	29			
20*		VGA-GREEN1	32			
21*		VGA-BLUE0	33			
22*		VGA-BLUE1	34			
23*		VGA-/HSYNC	36		PUSHB4	
26*		VGA-/VSYNC	37		PUSHB3	
27*	62	FLASH-A3	50	RAM-A0	LED2-B	IDE_DMARQ
28*	63	FLASH-A2, *PARPORT-S5	51	RAM-A10	LED2-E	/USB_INT
29*	64	FLASH-A1, *PARPORT-S4	56	RAM-A11	LED2-G	USB_SUSPEND
30*	19	SPARTAN-/WRITE	69		DIPSW1	
31*	15	SPARTAN-CS	68			/IDE_RESET
32	15*	SPARTAN-TDI	15			
34	19*	SPARTAN-TDO	30			
37	16	SPARTAN-CCLK	73			
38*	18	SPARTAN-DOUT/BSY	45	RAM-A1	LED2-DP	/IDE_DMACK
39*	2	FLASH-D0,DIN/D0,LED-S1	71	RAM-A16	BARLED-9	IDE_IORDY
40*	1	FLASH-A0, *PARPORT-S3	57	RAM-A9	LED2-C	IDE_INTRQ
41*	11	FLASH-/CE	65			
42**	57	FLASH-A10, *PARPORT-D2	58	RAM-A8	LED2-F	IDE_D8
43**	12	FLASH-/OE, *PARPORT-D7	61	/RAM-OE		IDE_D9
44*	4	FLASH-D1,LED-DP	40	RAM-D6	BARLED-2	IDE_D1
46*	5	FLASH-D2,LED-S4	39	RAM-D5	BARLED-3	IDE_D2
47**	43	FLASH-A11, *PARPORT-D3	59	RAM-A13	LED2-D	IDE_D10
48**	44	FLASH-A9, *PARPORT-D1	60	RAM-A15	LED2-A	IDE_D11
49*	6	FLASH-D3,LED-S6	38	RAM-D4	BARLED-4	IDE_D3
50**	45	FLASH-A8, *PARPORT-D0	78	RAM-A14	LED1-G	IDE_D12
51**	46	FLASH-A13, *PARPORT-D5	79	RAM-A12	LED1-B	IDE_D13
54*	47	FLASH-A14,DIPSW1A	82	RAM-A7	LED1-F	/IDE_CS0
56*	48	FLASH-A17,DIPSW1D	83	RAM-A6	LED1-A	/IDE_CS1
57*	7	FLASH-D4,LED-S5	35	RAM-D3	BARLED-5	IDE_D4
58**	49	FLASH-/WE, *PARPORT-D6	62	/RAM-WE	DIPSW2	IDE_D14
59*	50	FLASH-/RESET	66	AUDIO_LRCK	BARLED-10	
60*	8	FLASH-D5,LED-S3	80	RAM-D0	BARLED-7	IDE_D6,RS232_RD
62*	9	FLASH-D6,LED-S2	81	RAM-D1	BARLED-6	IDE_D5, RS232_CTS
63*	51	FLASH-A16,DIPSW1C	84	RAM-A5	LED1-DP	IDE_DA2
64*	52	FLASH-A15,DIPSW1B	3	RAM-A4	LED1-D	IDE_DA0
65**	56	FLASH-A12, *PARPORT-D4	4	RAM-A3	LED1-C	IDE_D15
66*	58	FLASH-A7	5	RAM-A2	DIPSW5	IDE_DA1
67*	10	FLASH-D7,LED-S0	10	RAM-D2	BARLED-8	IDE_D7
68*	38	SPARTAN-/INIT	41	RAM-D7	BARLED-1	IDE_D0
69	39	SPARTAN-/PROGRAM	55		PUSHB1	
72	40	SPARTAN-DONE	53			
74*	61	FLASH-A4	70	AUDIO_SDTI	DIPSW3	
75*	60	FLASH-A5	77	AUDIO_SCLK	DIPSW4	
76*	59	FLASH-A6	6	AUDIO_SDTO	LED1-E	
77*			9	AUDIO_MCLK	DIPSW6	
78*		PARPORT-S6	67		PUSHB2	
79*			7	/RAM_CE	DIPSW8	
80*			8		DIPSW7	RS232_RTS
83*			18			RS232_TD
84*			19			USB_SCL
85*			20			USB_SDA
86*			23			/IDE_DIOR

FPGA	CPLD	XSA Function	Proto. Pin	XStend V2.0 Functions		
87*			24			/IDE_DIOW
88	42	MASTER_CLK	13	MASTER_CLK		
91		SDRAM-CLK				
93*		PS2-DATA,PUSHBUTTON	25			
94*		PS2-CLK	26			
95		SDRAM-Q0				
96		SDRAM-Q15				
99		SDRAM-Q1				
100		SDRAM-Q14				
101		SDRAM-Q2				
102		SDRAM-Q13				
103		SDRAM-Q3				
106		SPARTAN-M2	12			
109	36	SPARTAN-M0	14			
111		SPARTAN-M1	21			
112		SDRAM-Q12				
113		SDRAM-Q4				
114		SDRAM-Q11				
115		SDRAM-Q5				
116		SDRAM-Q10				
117		SDRAM-Q6				
118		SDRAM-Q9				
120		SDRAM-Q7				
121		SDRAM-Q8				
122		SDRAM-QML				
123		SDRAM-/WE				
124		SDRAM-QMH				
126		SDRAM-/CAS				
129		SDRAM-CLK				
130		SDRAM-/RAS				
131		SDRAM-CKE				
132		SDRAM-/CS				
133		SDRAM-A12				
134		SDRAM-BA0				
136		SDRAM-A11				
137		SDRAM-BA1				
138		SDRAM-A9				
139		SDRAM-A10				
140		SDRAM-A8				
141		SDRAM-A0				
142	18*	SPARTAN-TMS	17			
	30	PARPORT-C1,CPLD-TCK				
	29	PARPORT-C2,CPLD-TMS				
	28	PARPORT-C3,CPLD-TDI				
	33	PARPORT-D0				
	32	PARPORT-D1				
	31	PARPORT-D2				
	27	PARPORT-D3				
	25	PARPORT-D4				
	24	PARPORT-D5				
	23	PARPORT-D6				
	22	PARPORT-D7				
	34	PARPORT-S3				
	20	PARPORT-S4				
	35	PARPORT-S5				
	53	PARPORT-S7,CPLD-TDO				
	17	PROG-OSC				
			64	Osc-In		USB_CLKOUT

B

XSA Schematics

The following pages show the detailed schematics for the XSA Board.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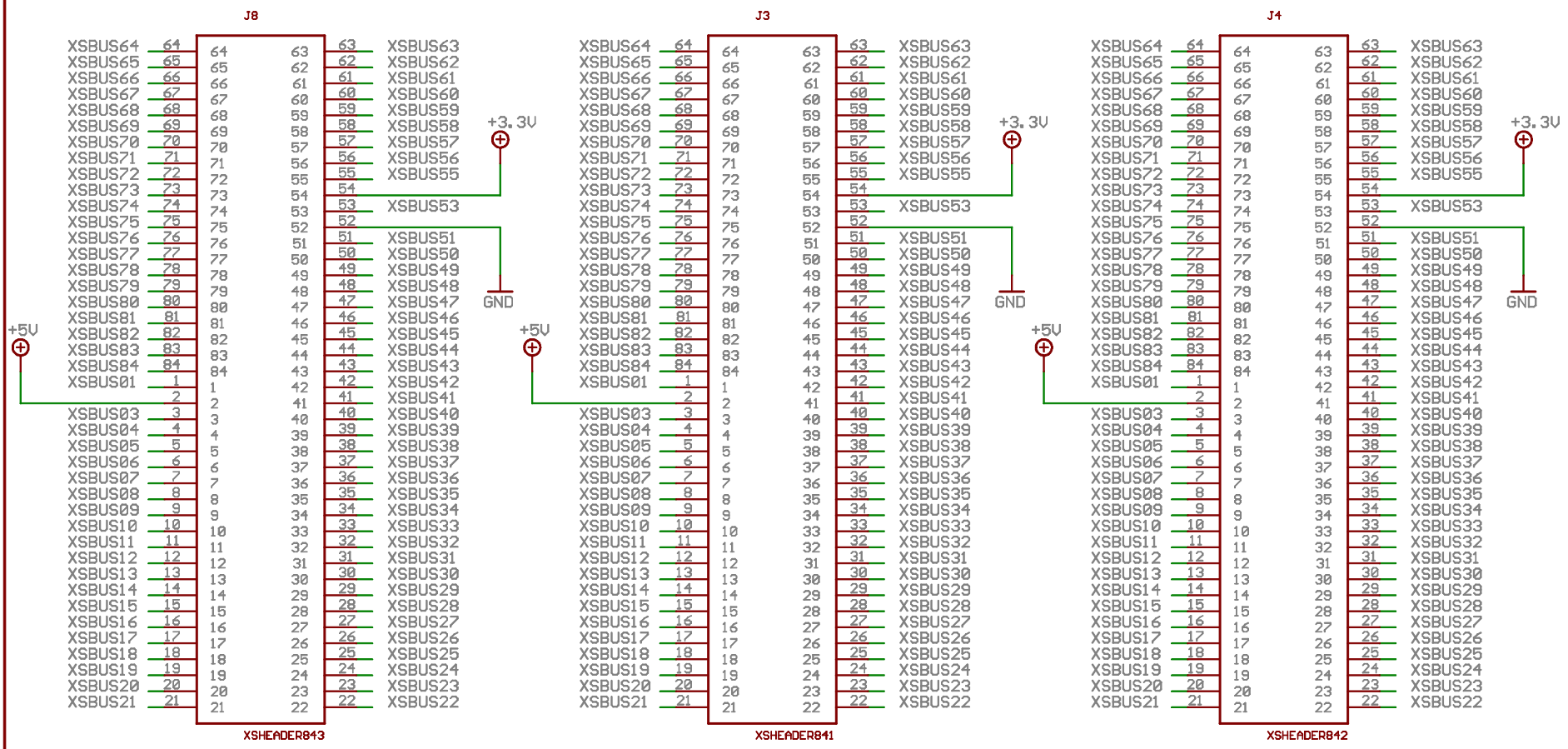
Date: 9/20/2002 02:54:02p
Sheet: 1/7
LM4808
LMV722
AOUTL
VCOM
AOUTR
VREFH
AINL-
AINL+
AINR-
AINR+
VREFL
/PWDA
/PWAD
CMODE
DEM0
DEM1
DIF0
DIF1
TST1
TST2
TST3
MCLK
SCLK
LRCK
SDTI
SDTO
DGND
AGND
AUDIO_MCLK
AUDIO_SCLK
AUDIO_LRCK
AUDIO_SDTI
AUDIO_SDTO
XSBUS09
XSBUS77
XSBUS66
XSBUS70
XSBUS06
FERRITE_BEAD
GND
+5V
+5V/1
+5V/2
VDD
VAA



XSA Mounting Socket and Daughterboard Conn.		
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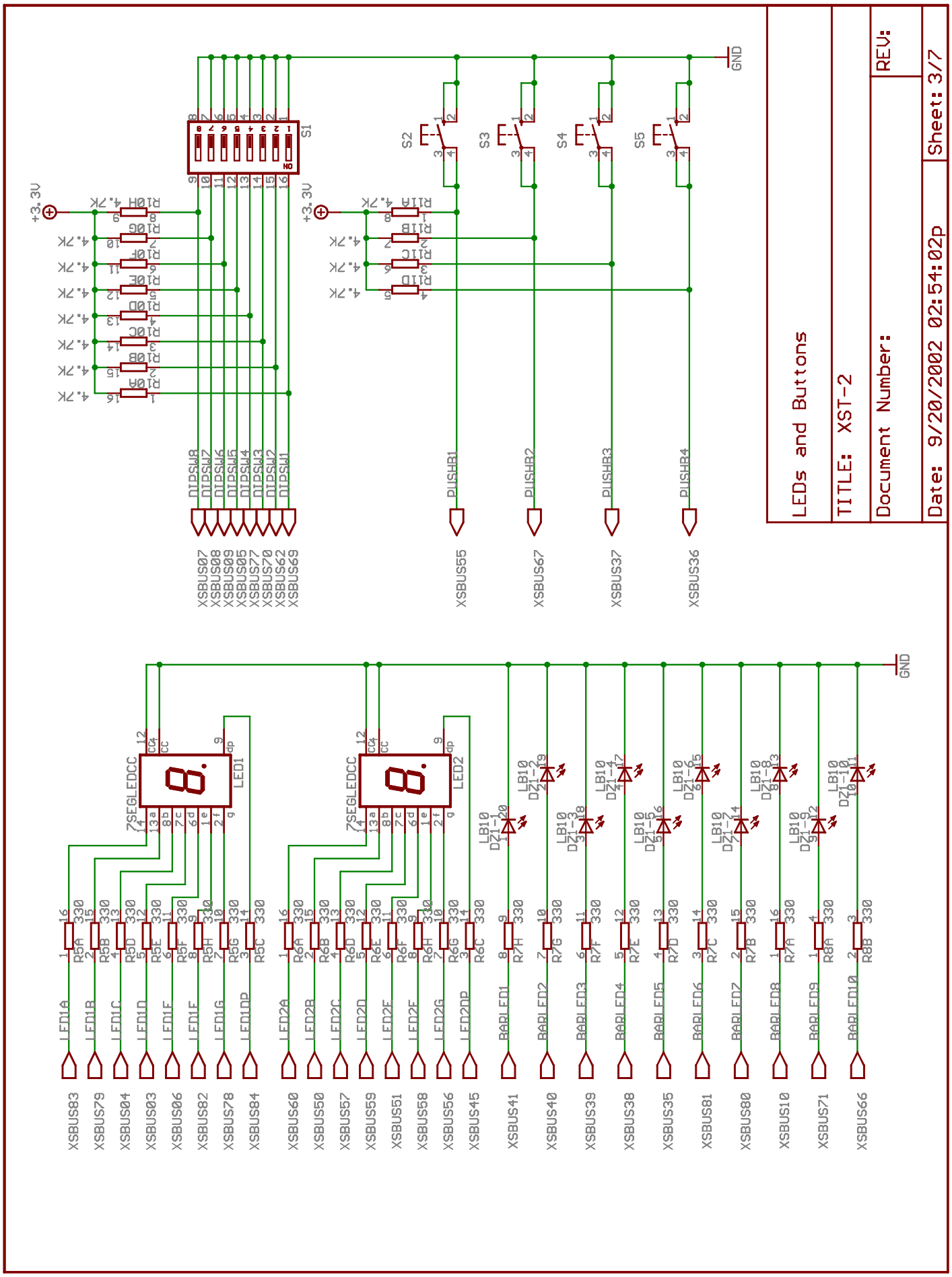
LEDs and Buttons
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Sheet: 3/7
+3.3V
GND
S1
S2
S3
S4
S5
4.7K
DIPSW1
DIPSW2
DIPSW3
DIPSW4
DIPSW5
DIPSW6
DIPSW7
DIPSW8
PUSHB1
PUSHB2
PUSHB3
PUSHB4
XSBUS07
XSBUS08
XSBUS09
XSBUS05
XSBUS77
XSBUS70
XSBUS62
XSBUS69
XSBUS55
XSBUS67
XSBUS37
XSBUS36
7SEGLEDCC
LED1
LED2
330
LB10
LED1A
LED1B
LED1C
LED1D
LED1E
LED1F
LED1G
LED1DP
LED2A
LED2B
LED2C
LED2D
LED2E
LED2F
LED2G
LED2DP
BARLED1
BARLED2
BARLED3
BARLED4
BARLED5
BARLED6
BARLED7
BARLED8
BARLED9
BARLED10
XSBUS83
XSBUS79
XSBUS04
XSBUS03
XSBUS06
XSBUS82
XSBUS78
XSBUS84
XSBUS60
XSBUS50
XSBUS57
XSBUS59
XSBUS51
XSBUS58
XSBUS56
XSBUS45
XSBUS41
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XSBUS38
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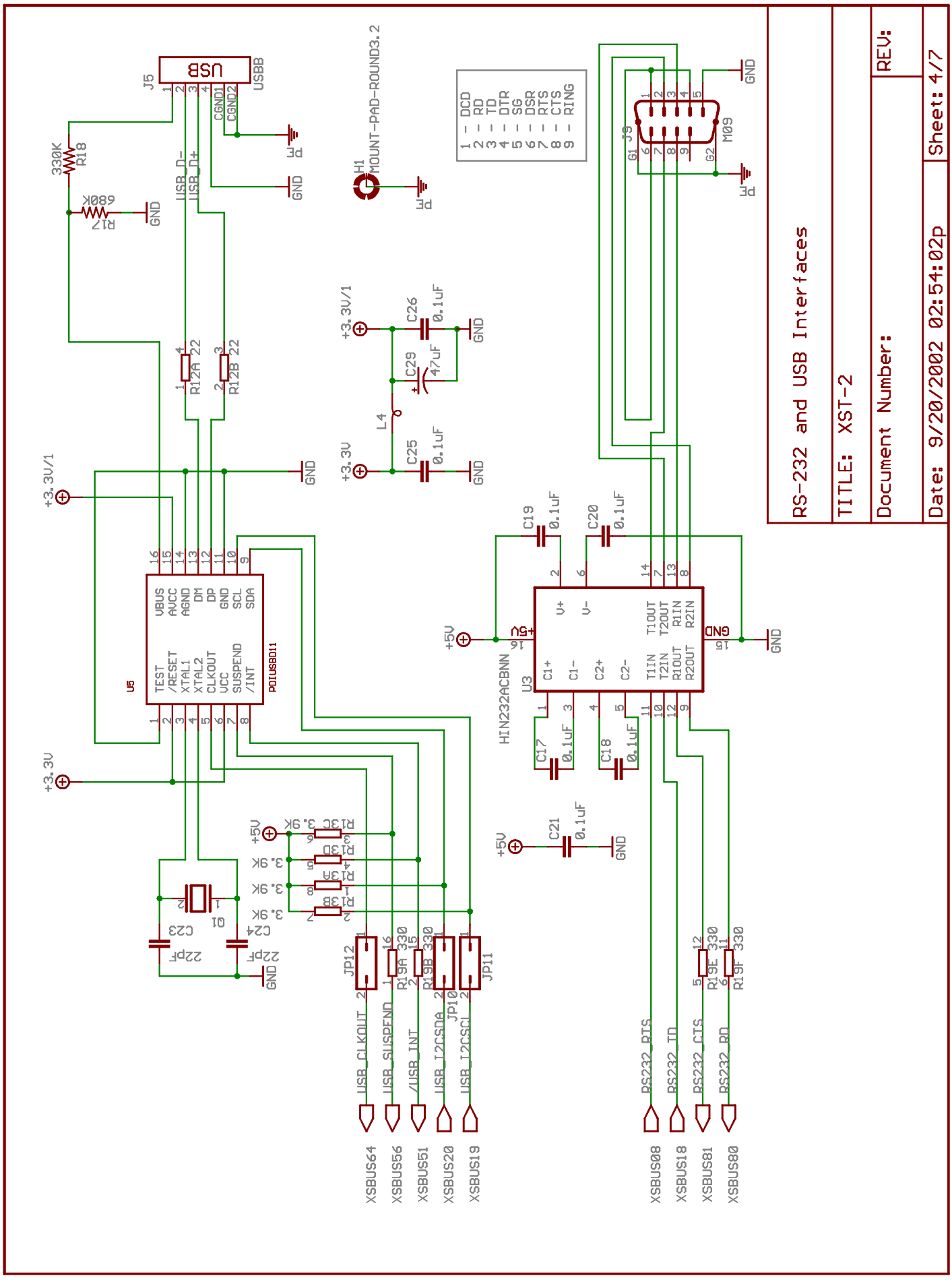
XSBUS81
XSBUS80
XSBUS10
XSBUS71
XSBUS66


RS-232 and USB Interfaces
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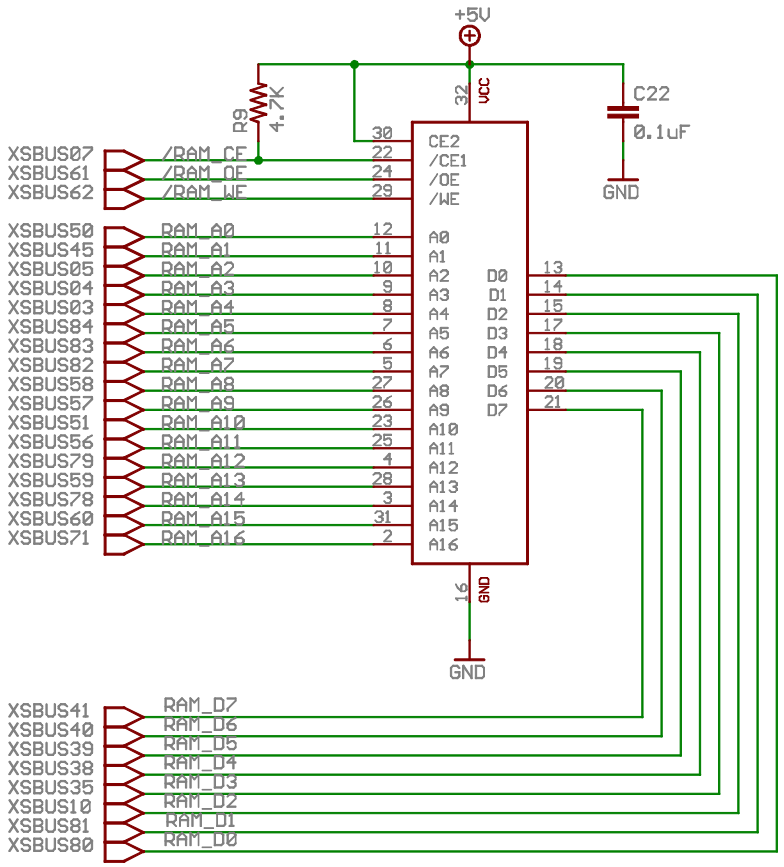
Date: 9/20/2002 02:54:02p
Sheet: 4/7
USB
USBB
J5
USB_D-
USB_D+
330K
R18
680K
R17
GND
+5V
H1
MOUNT-PAD-ROUND3.2
1 - DCD
2 - RD
3 - TD
4 - DTR
5 - SG
6 - DSR
7 - RTS
8 - CTS
9 - RING
J9
M09
R12A 22
R12B 22
+3.3V/1
+3.3V
C26 0.1uF
C29 47uF
C25 0.1uF
L4
U5
PDIUSBD11
VBUS
AVCC
AGND
DM
DP
GND
SCL
SDA
TEST
/RESET
XTAL1
XTAL2
CLKOUT
VCC
SUSPEND
/INT
U3
HIN232ACBNN
C1+
C1-
C2+
C2-
V+
V-
T1IN
T2IN
R1OUT
R2OUT
T1OUT
T2OUT
R1IN
R2IN
C17 0.1uF
C18 0.1uF
C19 0.1uF
C20 0.1uF
C21 0.1uF
Q1
C23 22pF
C24 22pF
3.9K
JP12
JP10
JP11
R19A 330
R19B 330
R19E 330
R19F 330
USB_CLKOUT
USB_SUSPEND
/USB_INT
USB_I2CSDA
USB_I2CSCL
RS232_RTS
RS232_TD
RS232_CTS
RS232_RD
XSBUS64
XSBUS56
XSBUS51
XSBUS20
XSBUS19
XSBUS08
XSBUS18
XSBUS81
XSBUS80



SRAM		
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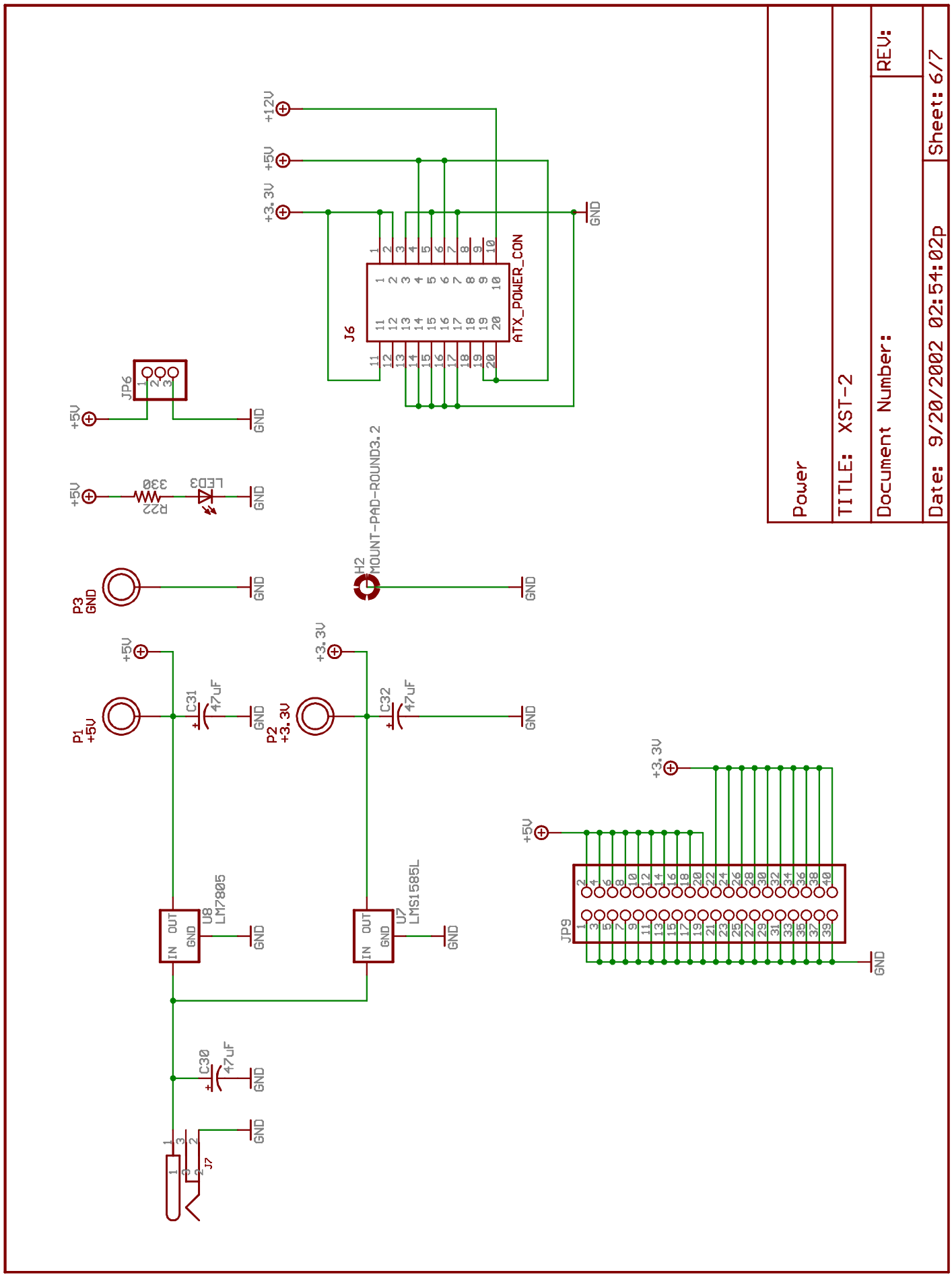
Power
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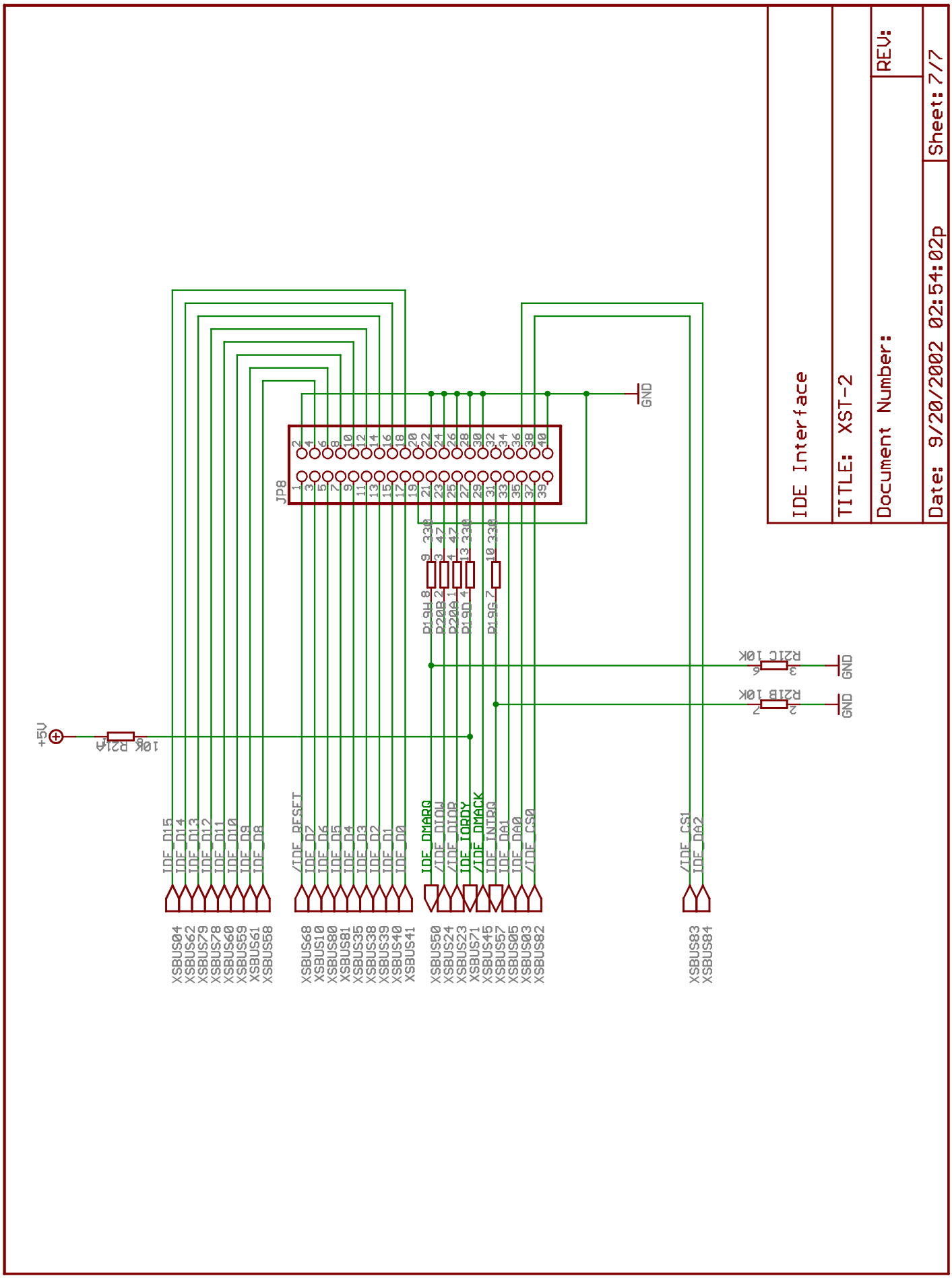
Sheet: 6/7
+12V
+5V
+3.3V
GND
J6
ATX_POWER_CON
JP6
LED3
R22
330
H2
MOUNT-PAD-ROUND3.2
P3
GND
P1
+5V
P2
+3.3V
C31
47uF
C32
47uF
C30
47uF
U8
LM7805
U7
LM1585L
IN
OUT
J7
JP9


IDE Interface
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Sheet: 7/7
JP8
GND
+5V
10K R21A
R19H 8 330
R20B 2 47
R20A 1 47
R19D 4 330
R19G 7 330
R21C 10K
R21B 10K
IDE_D15
IDE_D14
IDE_D13
IDE_D12
IDE_D11
IDE_D10
IDE_D9
IDE_D8
/IDE_RESET
IDE_D7
IDE_D6
IDE_D5
IDE_D4
IDE_D3
IDE_D2
IDE_D1
IDE_D0
IDE_DMARQ
/IDE_DIOW
/IDE_DIOR
IDE_IORDY
/IDE_DMACK
IDE_INTRQ
IDE_DA1
IDE_DA0
/IDE_CS0
/IDE_CS1
IDE_DA2
XSBUS04
XSBUS62
XSBUS79
XSBUS78
XSBUS60
XSBUS59
XSBUS61
XSBUS58
XSBUS68
XSBUS10
XSBUS80
XSBUS81
XSBUS35
XSBUS38
XSBUS39
XSBUS40
XSBUS41
XSBUS50
XSBUS24
XSBUS23
XSBUS71
XSBUS45
XSBUS57
XSBUS05
XSBUS03
XSBUS82
XSBUS83
XSBUS84

A

XSV Pin Connections

The following tables list the pin numbers of the Virtex FPGA and the XC95108 CPLD along with the pin names of the other chips that they connect to. These connections correspond with the pin assignments in the user-constraint files VIRTEX.UCF and CPLD.UCF.

Connections Between the Virtex FPGA and the Other XSV Board Components

Virtex FPGA		XC95108 CPLD	LEDs	Switches	Flash RAM	Ethernet	Video Decoder	RAMDAC	Codec	RAM	PS/2	USB	Parallel Port	Serial Port	Prog. Osc.	Xchecker
1	GND															
2	TMS	35	S3 (left)		D3											TMS
3									MCLK							
4									LRCK							
5									SCLK							
6									SDIN							
7									SDOUT							
8	GND															
9												VM				
10												VP				
11												RCV				
12												/OE				
13											CLK	VPO				
14	GND															
15	VCCO															
16	VCCINT															
17											DATA	VMO				
18						FDS/MDINT										
19						MDC										
20						MDIO										
21						CRS										
22	GND															
23						COL										
24						TRSTE										
25						TxEN										
26						RxDV		RS2								
27						TxERR										
28						RxERR		RS1								
29	GND															
30	VCCO															
31						TxD4		RS0								
32	VCCINT															
33						RxD4										
34						RxD3		D7								
35						RxD2		D6								
36						RxD1		D5								
37	GND															
38						RxD0		D4								
39						TxD3		D3								
40						TxD2		D2								
41						TxD1		D1								
42						TxD0		D0								
43	VCCINT															
44	VCCO															
45	GND															

Connections Between the Virtex FPGA and the Other XSV Board Components

Virtex FPGA		XC95108 CPLD	LEDs	Switches	Flash RAM	Ethernet	Video Decoder	RAMDAC	Codec	RAM	PS/2	USB	Parallel Port	Serial Port	Prog. Osc.	Xchecker
46								/WR								
47								/RD								
48								/HSYNC								
49								/VSYNC								
50								/BLANK								
51	GND															
52								PIXELCLK								
53										A9 (right)						
54										A8 (right)						
55										A7 (right)						
56										A6 (right)						
57										A5 (right)						
58	M1	14														
59	GND															
60	M0	13														
61	VCCO															
62	M2	15														
63										A4 (right)						
64										A3 (right)						
65										A2 (right)						
66										A1 (right)						
67										A0 (right)						
68										/WE (right)						
69	GND															
70								P0		D0 (right)						
71								P1		D1 (right)						
72								P2		D2 (right)						
73								P3		D3 (right)						
74								P4		D4 (right)						
75	GND															
76	VCCO															
77	VCCINT															
78								P5		D5 (right)						
79								P6		D6 (right)						
80								P7		D7 (right)						
81										D8 (right)						
82										D9 (right)						
83	GND															
84										D10 (right)						
85										D11 (right)						
86										D12 (right)						
87										D13 (right)						
88	VCCINT															
89	PGCK	22													CLK	CLKI
90	VCCO															

Connections Between the Virtex FPGA and the Other XSV Board Components

Virtex FPGA		XC95108 CPLD	LEDs	Switches	Flash RAM	Ethernet	Video Decoder	RAMDAC	Codec	RAM	PS/2	USB	Parallel Port	Serial Port	Prog. Osc.	Xchecker
91	GND															
92	PGCK						LLCK									
93										D14 (right)						
94										D15 (right)						
95										/OE (right)						
96										A18 (right)						
97										A17 (right)						
98	GND															
99										A16 (right)						
100										A15 (right)						
101										A14 (right)						
102										A13 (right)						
103										A12 (right)						
104	VCCINT															
105	VCCO															
106	GND															
107										A11 (right)						
108										A10 (right)						
109										/CE (right)						
110							RTS1									
111							RTS0									
112	GND															
113							RTC0									
114							SCL									
115							SDA									
116							VPO0									
117							VPO1									
118							VPO2									
119	GND															
120	DONE	10														DONE
121	VCCO															
122	/PROG	11														/PROGRAM
123	/INIT	9														/INIT
124	D7	40	S0 (right)		D7											
125							VPO3									
126							VPO4									
127							VPO5									
128							VPO6									
129	GND															
130							VPO7									
131		43	BAR8		/WE											
132		16	S1 (right)		A0											RT
133		17	S2 (right)		A1											RD
134	D6	39	S6 (left)		D6											
135	GND															

Connections Between the Virtex FPGA and the Other XSV Board Components

Virtex FPGA		XC95108 CPLD	LEDs	Switches	Flash RAM	Ethernet	Video Decoder	RAMDAC	Codec	RAM	PS/2	USB	Parallel Port	Serial Port	Prog. Osc.	Xchecker
136	VCCO															
137	VCCINT															
138	D5	37	S5 (left)		D5											
139		18	S3 (right)		A2											TRIG
140		59		DIPSW8	A20											
141		19	S4 (right)		A3											CLKO
142		58		DIPSW7	A19											
143	GND															
144		20	S5 (right)		A4											RST
145	D4	36	S4 (left)		D4											
146		56		DIPSW6	A18											
147		23	S6 (right)		A5											
148	VCCINT															
149		55		DIPSW5	A17											
150	VCCO															
151	GND															
152		24	BAR0		A6											
153		54		DIPSW4	A16											
154		25	BAR1		A7											
155		53		DIPSW3	A15											
156	D3	35	S3 (left)		D3											TMS
157		27	BAR2		A8											
158	GND															
159		52		DIPSW2	A14											
160		28	BAR3		A9											
161		50		DIPSW1	A13											
162		29	BAR4		A10											
163	D2	34	S2 (left)		D2											
164	VCCINT															
165	VCCO															
166	GND															
167	D1	33	S1 (left)		D1											TDI
168		49	BAR6		A12											
169		30	BAR5		A11											
170		46			/CE											
171		41	BAR9		RDY											
172	GND															
173		42	BAR7		/OE											
174				SW1												
175				SW2												
176				SW3								SUSPND				
177	D0/DIN	32	S0 (left)		D0											DIN
178	BUSY/DC	6														
179	CCLK	12														CCLK
180	VCCO															

Connections Between the Virtex FPGA and the Other XSV Board Components

Virtex FPGA		XC95108 CPLD	LEDs	Switches	Flash RAM	Ethernet	Video Decoder	RAMDAC	Codec	RAM	PS/2	USB	Parallel Port	Serial Port	Prog. Osc.	Xchecker
181	TDO	34	S2 (left)		D2											
182	GND															
183	TDI	33	S1 (left)		D1											TDI
184	/CS	8														
185	/WR	7		SW4												
186										/CE (left)						
187										A9 (left)						
188										A8 (left)						
189										A7 (left)						
190	GND															
191										A6 (left)						
192										A5 (left)						
193										A4 (left)						
194										A3 (left)						
195										A2 (left)						
196	GND															
197	VCCO															
198	VCCINT															
199										A1 (left)						
200										A0 (left)						
201										/WE (left)						
202										D0 (left)						
203										D1 (left)						
204	GND															
205										D2 (left)						
206										D3 (left)						
207										D4 (left)						
208										D5 (left)						
209										D6 (left)						
210	PGCK					TxCLK										
211	GND															
212	VCCO															
213	PGCK					RxCLK										
214	VCCINT															
215										D7 (left)						
216										D8 (left)						
217										D9 (left)						
218										D10 (left)						
219	GND															
220										D11 (left)						
221										D12 (left)						
222										D13 (left)						
223										D14 (left)						
224										D15 (left)						
225	VCCINT															

Connections Between the Virtex FPGA and the Other XSV Board Components

Virtex FPGA		XC95108 CPLD	LEDs	Switches	Flash RAM	Ethernet	Video Decoder	RAMDAC	Codec	RAM	PS/2	USB	Parallel Port	Serial Port	Prog. Osc.	Xchecker
226	VCCO															
227	GND															
228										/OE (left)						
229										A18 (left)						
230										A17 (left)						
231										A16 (left)						
232										A15 (left)						
233	GND															
234										A14 (left)						
235										A13 (left)						
236										A12 (left)						
237										A11 (left)						
238										A10 (left)						
239	TCK	4														TCK
240	VCCO															

Connections Between the XC95108 CPLD and the Other XSV Board Components

XC95108 CPLD		Virtex FPGA	LEDs	Switches	Flash RAM	Ethernet	Video Decoder	RAMDAC	Codec	RAM	PS/2	USB	Parallel Port	Serial Port	Prog. Osc.	Xchecker
1						/LEDS										
2						CFG1										
3					/RESET	/RESET	CE									
4		239														TCK
5	VCCINT															
6		178														
7		185		SW4												
8		184														
9		123														/INIT
10		120														DONE
11		122														/PROGRA
12		179														CCLK
13		60														
14		58														
15		62														
16		132	S1 (right)		A0											RT
17		133	S2 (right)		A1											RD
18		139	S3 (right)		A2											TRIG
19		141	S4 (right)		A3											CLKO
20		144	S5 (right)		A4											
21	GND															
22	PGCK	89													CLK	CLKI
23	PGCK	147	S6 (right)		A5											
24		152	BAR0		A6											
25		154	BAR1		A7											
26	VCCO															
27	PGCK	157	BAR2		A8											
28		160	BAR3		A9											
29		162	BAR4		A10											
30		169	BAR5		A11											
31	GND															
32		177	S0 (left)		D0											DIN
33		167,183	S1 (left)		D1											TDI
34		163,181	S2 (left)		D2											
35		156,2	S3 (left)		D3											TMS
36		145	S4 (left)		D4											
37		138	S5 (left)		D5											
38	VCCO															
39		134	S6 (left)		D6											
40		124	S0 (right)		D7											
41		171	BAR9		RDY											
42		173	BAR7		/OE											

Connections Between the XC95108 CPLD and the Other XSV Board Components

XC95108 CPLD		Virtex FPGA	LEDs	Switches	Flash RAM	Ethernet	Video Decoder	RAMDAC	Codec	RAM	PS/2	USB	Parallel Port	Serial Port	Prog. Osc.	Xchecker
43		131	BAR8		/WE											
44	GND															
45	TDI												C3			
46		170			/CE											
47	TMS												C2			
48	TCK												C1			
49		168	BAR6		A12											
50		161		DIPSW1	A13											
51	VCCO															
52		159		DIPSW2	A14											
53		155		DIPSW3	A15											
54		153		DIPSW4	A16											
55		149		DIPSW5	A17											
56		146		DIPSW6	A18											
57	VCCINT															
58		142		DIPSW7	A19											
59		140		DIPSW8	A20											
60													S4			
61													S5			
62	GND															
63													S7			
64													S6			
65													D7			
66													D6			
67													D5			
68													D4			
69	GND															
70													D3			
71													C3			
72													D2			
73													C2			
74													D1			
75	GND															
76													S3			
77													D0			
78													C1			
79													C0			
80														RxD		
81														TxD		
82														RTS		
83	TDO												S7			
84	GND															

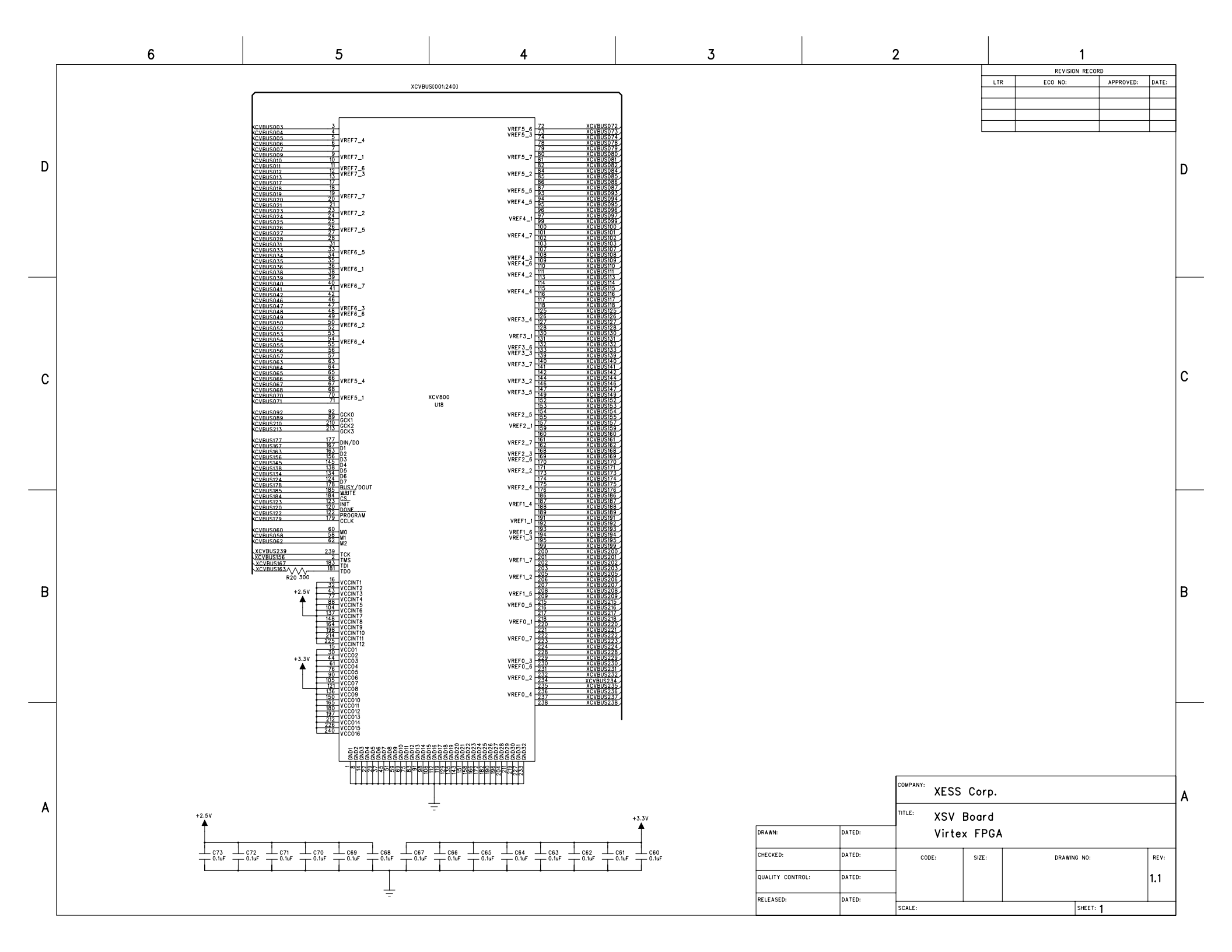
Connections Between the XC95108 CPLD and the Other XSV Board Components

XC95108 CPLD		Virtex FPGA	LEDs	Switches	Flash RAM	Ethernet	Video Decoder	RAMDAC	Codec	RAM	PS/2	USB	Parallel Port	Serial Port	Prog. Osc.	Xchecker
85														CTS		
86						MF4										
87						MF3										
88	VCCO															
89						MF2										
90						MF1										
91						MF0										
92						FDE										
93						CFG0										
94						MDDIS										
95						/LEDR										
96						/LEDT										
97						/LEDL										
98	VCCINT															
99						/LEDC										
100	GND															

B

XSV Schematics

The following pages show the detailed schematics for the XSV Board.



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CHECKED:	DATED:
QUALITY CONTROL:	DATED:
RELEASED:	DATED:
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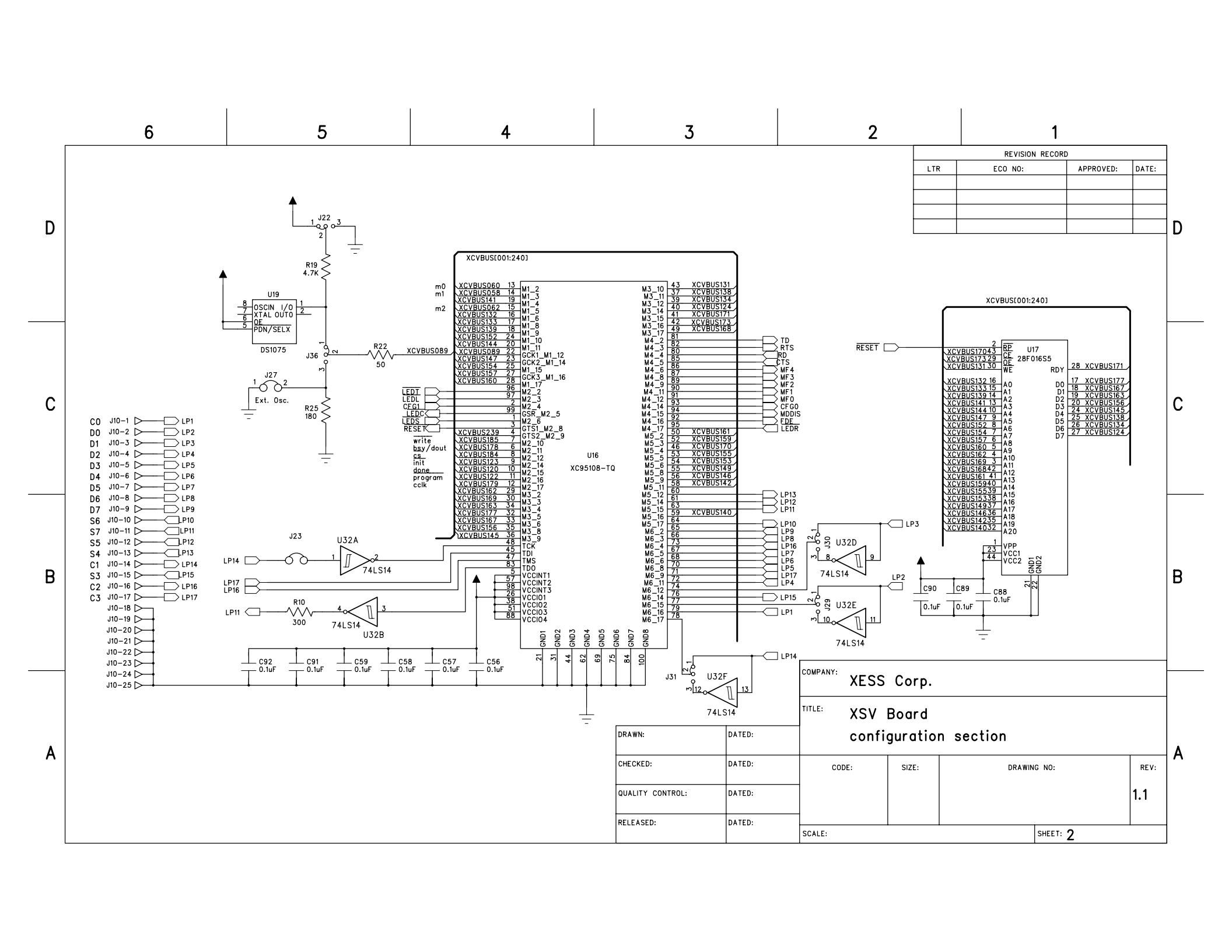
REV:	1.1
SCALE:	
SHEET:	1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APPROVED:
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28F016S5
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DS1075
Ext. Osc.
74LS14
U32A
U32B
U32D
U32E
U32F
XCVBUS[001:240]
C0 J10-1 LP1
D0 J10-2 LP2
D1 J10-3 LP3
D2 J10-4 LP4
D3 J10-5 LP5
D4 J10-6 LP6
D5 J10-7 LP7
D6 J10-8 LP8
D7 J10-9 LP9
S6 J10-10 LP10
S7 J10-11 LP11
S5 J10-12 LP12
S4 J10-13 LP13
C1 J10-14 LP14
S3 J10-15 LP15
C2 J10-16 LP16
C3 J10-17 LP17
J10-18
J10-19
J10-20
J10-21
J10-22
J10-23
J10-24
J10-25
R19 4.7K
R22 50
R25 180
R10 300
C92 0.1uF
C91 0.1uF
C59 0.1uF
C58 0.1uF
C57 0.1uF
C56 0.1uF
C90 0.1uF
C89 0.1uF
C88 0.1uF
COMPANY: XESS Corp.
TITLE: XSV Board configuration section
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DATED:
CHECKED:
QUALITY CONTROL:
RELEASED:
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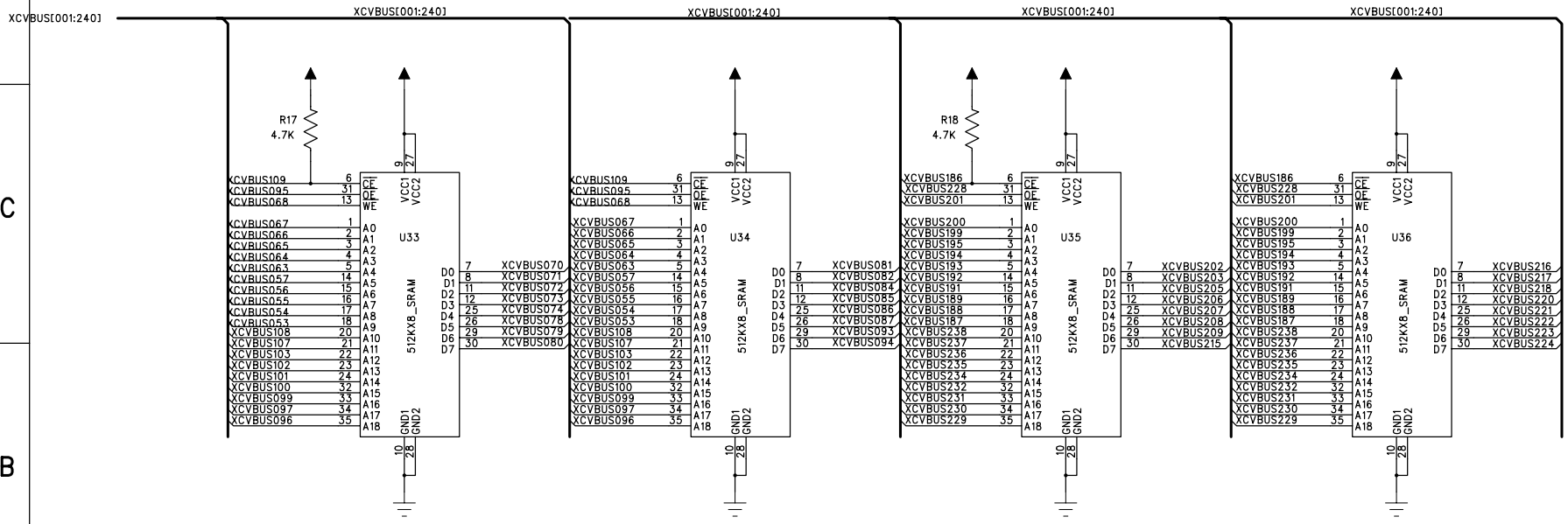

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QUALITY CONTROL:	DATED:
RELEASED:	DATED:

COMPANY: XESS Corp.

TITLE: XSV Board
RAM section

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SCALE:

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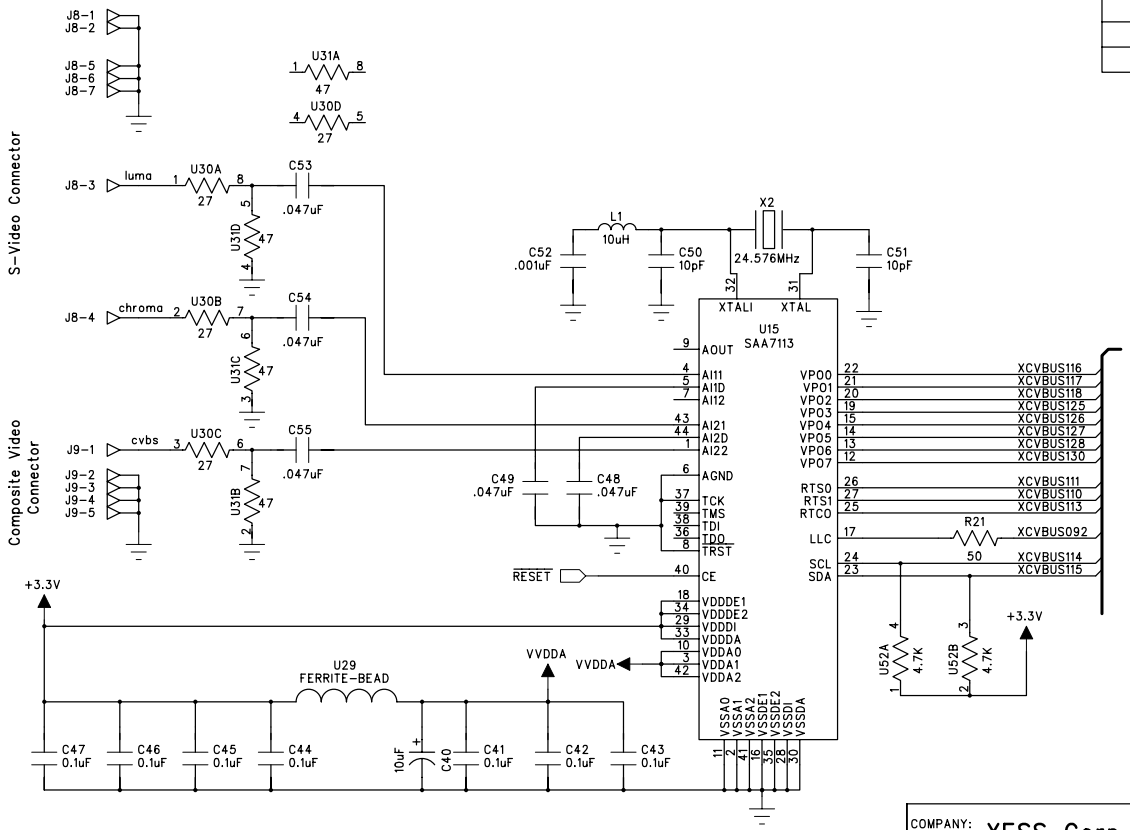

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DRAWN:	DATED:
CHECKED:	DATED:
QUALITY CONTROL:	DATED:
RELEASED:	DATED:

COMPANY: XESS Corp.

TITLE: XSV Board
video decoder section

CODE:	SIZE:	DRAWING NO:	REV:
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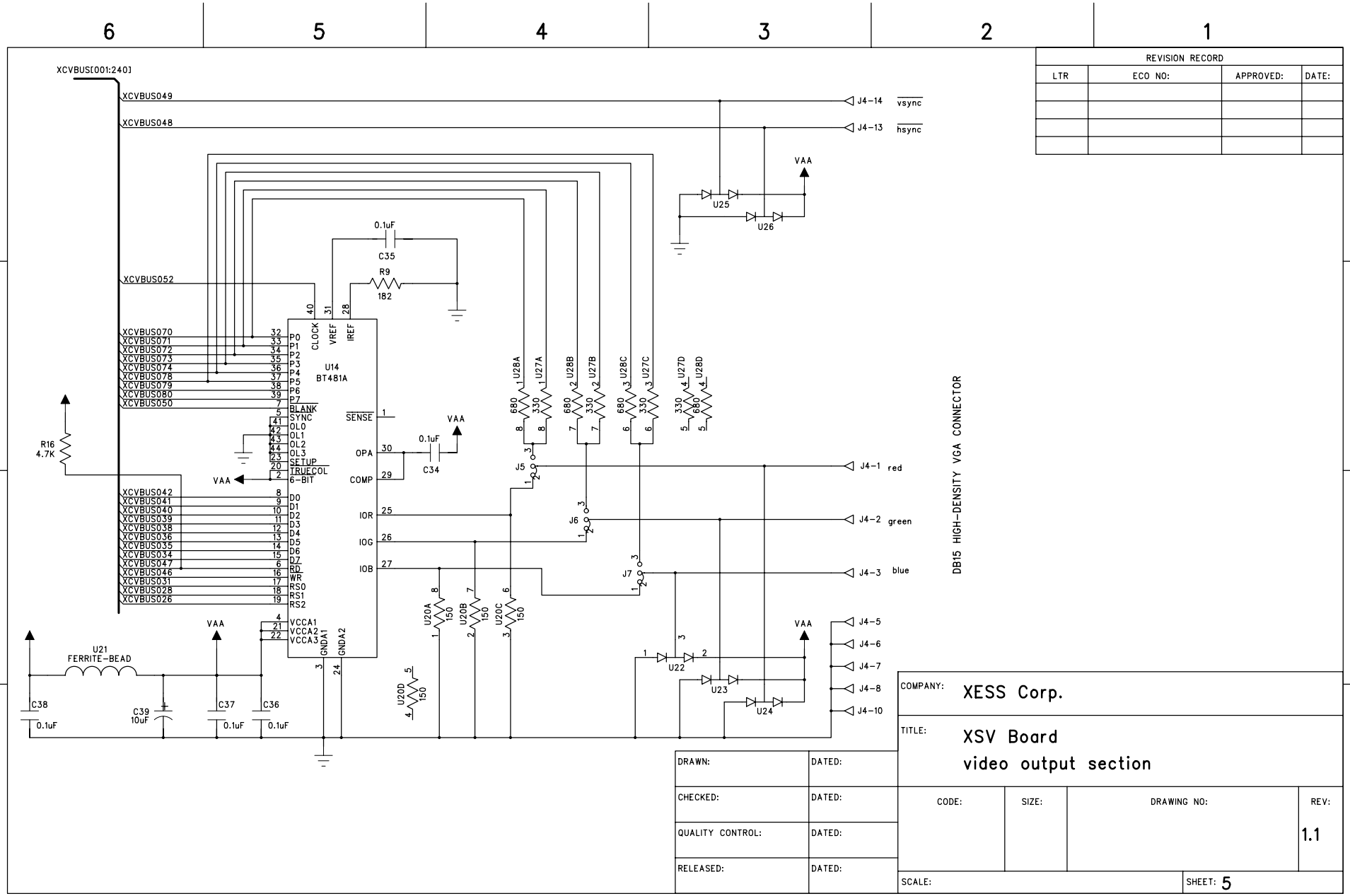
SCALE:

SHEET: 4



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DRAWN:	DATED:
CHECKED:	DATED:
QUALITY CONTROL:	DATED:
RELEASED:	DATED:

COMPANY: XESS Corp.

TITLE: XSV Board
video output section

CODE:	SIZE:	DRAWING NO:	REV:
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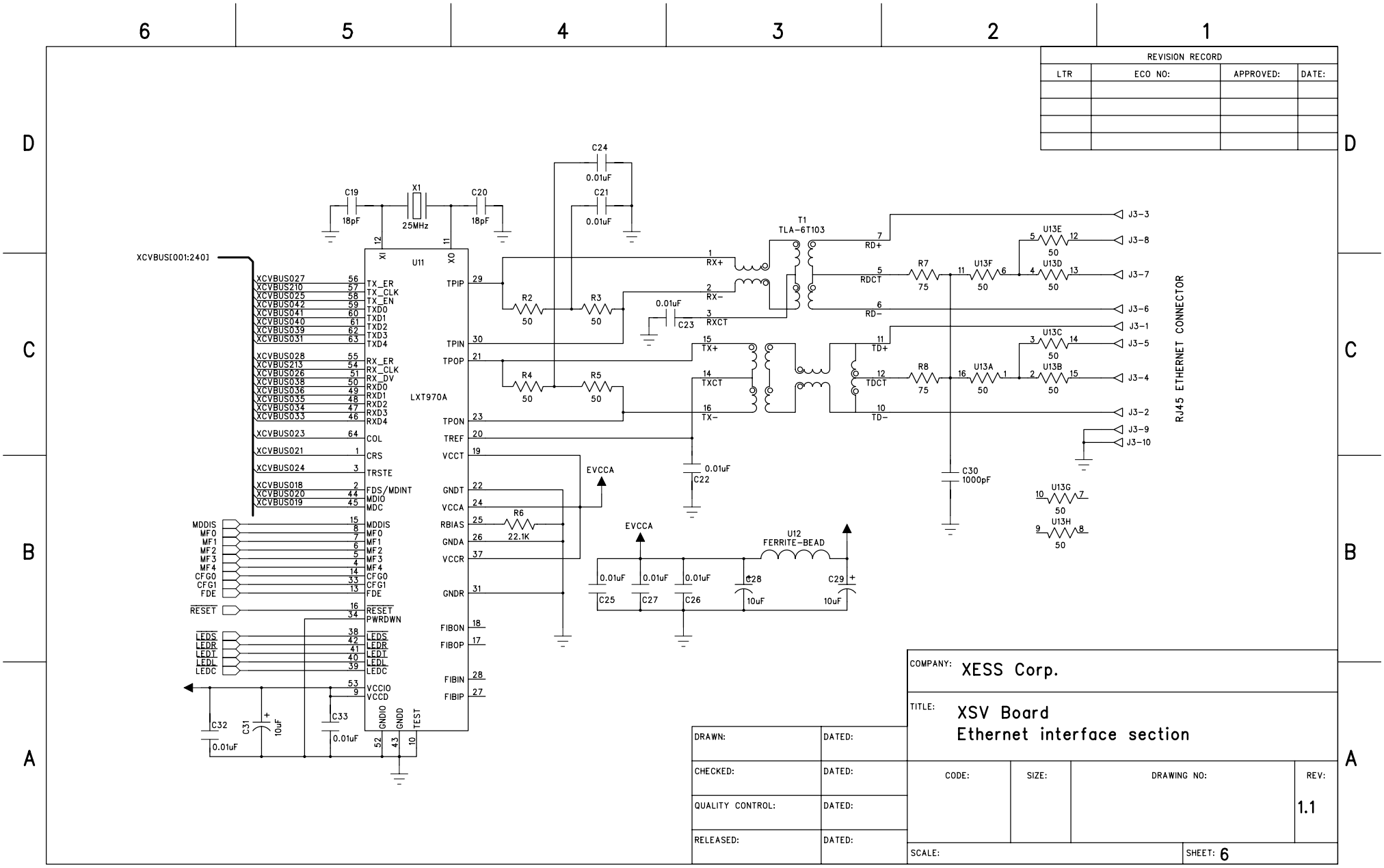
SCALE:

SHEET: 5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APPROVED:
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LXT970A
XCVBUS[001:240]
X1
25MHz
C19
18pF
C20
18pF
C24
0.01uF
C21
0.01uF
T1
TLA-6T103
RJ45 ETHERNET CONNECTOR
J3-1
J3-2
J3-3
J3-4
J3-5
J3-6
J3-7
J3-8
J3-9
J3-10
R2
50
R3
50
R4
50
R5
50
R6
22.1K
R7
75
R8
75
C22
0.01uF
C23
0.01uF
C30
1000pF
EVCCA
U12
FERRITE-BEAD
C25
0.01uF
C27
0.01uF
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0.01uF
C28
10uF
C29
10uF
C31
10uF
C32
0.01uF
C33
0.01uF
COMPANY: XESS Corp.
TITLE: XSV Board
Ethernet interface section
DRAWN:
DATED:
CHECKED:
DATED:
QUALITY CONTROL:
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DATED:
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REV:
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SCALE:
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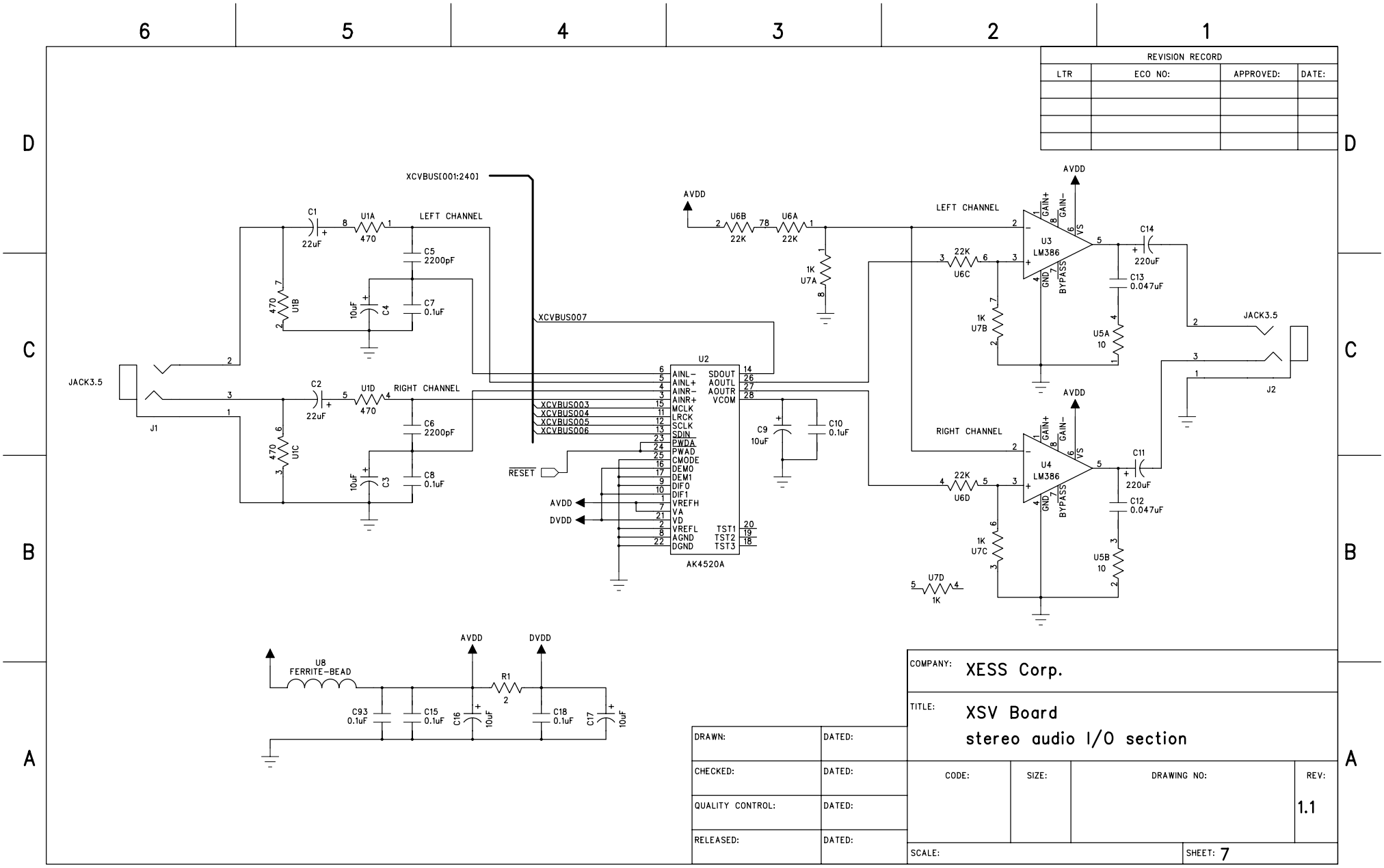
6
5
4
3
2
1
D
C
B
A
REVISION RECORD
LTR
ECO NO:
APPROVED:
DATE:
XCVBUS[001:240]
JACK3.5
J1
C1
22uF
U1A
470
LEFT CHANNEL
C5
2200pF
C7
0.1uF
C4
10uF
U1B
470
C2
22uF
U1D
470
RIGHT CHANNEL
C6
2200pF
C8
0.1uF
C3
10uF
U1C
470
XCVBUS007
XCVBUS003
XCVBUS004
XCVBUS005
XCVBUS006
RESET
U2
AINL−
AINL+
AINR−
AINR+
MCLK
LRCK
SCLK
SDIN
PWDA
PWAD
CMODE
DEM0
DEM1
DIF0
DIF1
VREFH
VA
VD
VREFL
AGND
DGND
SDOUT
AOUTL
AOUTR
VCOM
TST1
TST2
TST3
AK4520A
AVDD
DVDD
C9
10uF
C10
0.1uF
U6B
22K
U6A
22K
U7A
1K
LEFT CHANNEL
U3
LM386
GAIN+
GAIN−
VS
BYPASS
GND
U6C
22K
U7B
1K
C14
220uF
C13
0.047uF
U5A
10
JACK3.5
J2
RIGHT CHANNEL
U4
LM386
U6D
22K
U7C
1K
C11
220uF
C12
0.047uF
U5B
10
U7D
1K
U8
FERRITE−BEAD
R1
2
C93
0.1uF
C15
0.1uF
C16
10uF
C18
0.1uF
C17
10uF
DRAWN:
DATED:
CHECKED:
DATED:
QUALITY CONTROL:
DATED:
RELEASED:
DATED:
COMPANY:
XESS Corp.
TITLE:
XSV Board
stereo audio I/O section
CODE:
SIZE:
DRAWING NO:
REV:
1.1
SCALE:
SHEET: 7

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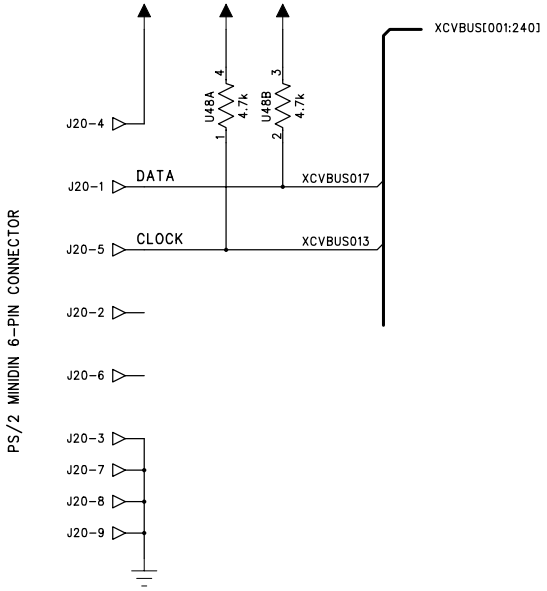

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CHECKED:	DATED:
QUALITY CONTROL:	DATED:
RELEASED:	DATED:

COMPANY: XESS Corp.

TITLE: XSV Board
PS/2 interface section

CODE:	SIZE:	DRAWING NO:	REV:
			1.1

SCALE:

SHEET: 8

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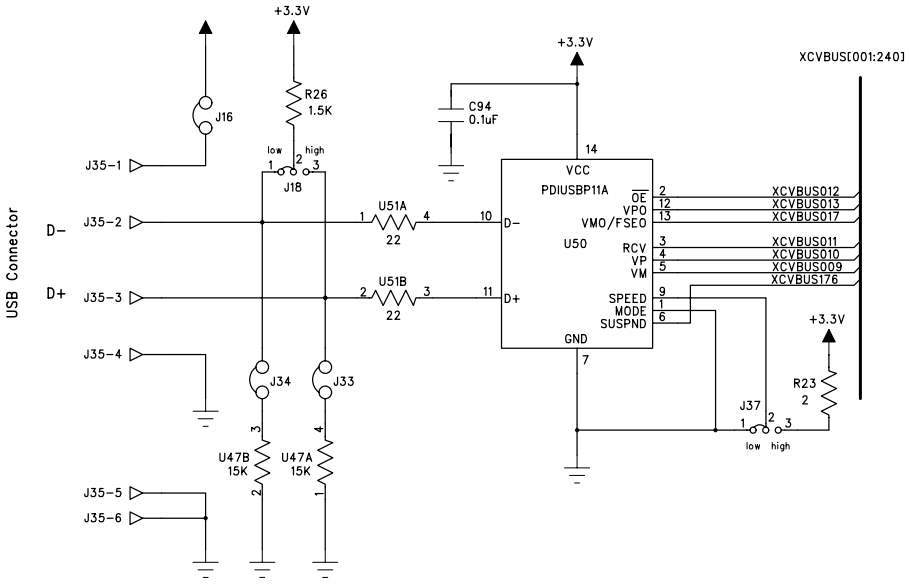

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CHECKED:	DATED:
QUALITY CONTROL:	DATED:
RELEASED:	DATED:

COMPANY: XESS Corp.

TITLE: XSV Board
USB interface section

CODE:	SIZE:	DRAWING NO:	REV:
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SCALE:

SHEET: 9

REVISION RECORD			
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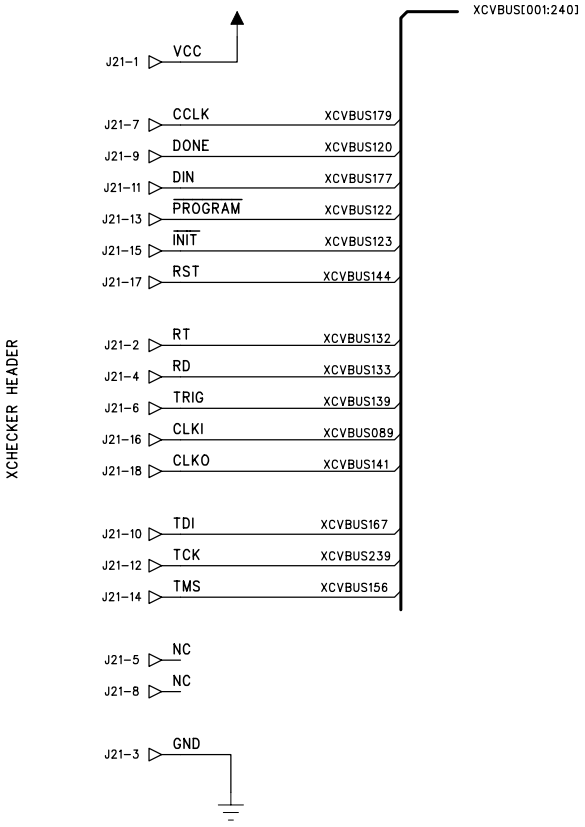


DRAWN:	DATED:
CHECKED:	DATED:
QUALITY CONTROL:	DATED:
RELEASED:	DATED:

COMPANY: XESS Corp.

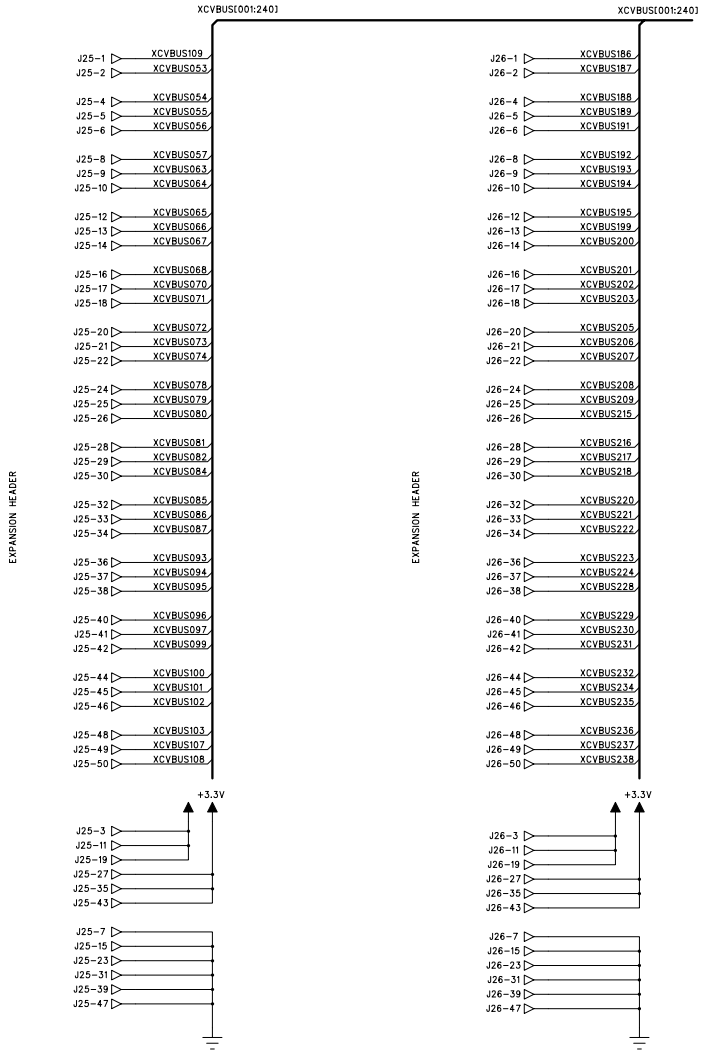
TITLE: XSV Board
XCHECKER interface section

CODE:	SIZE:	DRAWING NO:	REV:
			1.1

SCALE:

SHEET: 10

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:



DRAWN:	DATED:	COMPANY: XESS Corp.			
CHECKED:	DATED:	TITLE: XSV Board expansion interface section			
QUALITY CONTROL:	DATED:	CODE:	SIZE:	DRAWING NO:	REV: 1.1
RELEASED:	DATED:	SCALE:		SHEET: 11	

REVISION RECORD			
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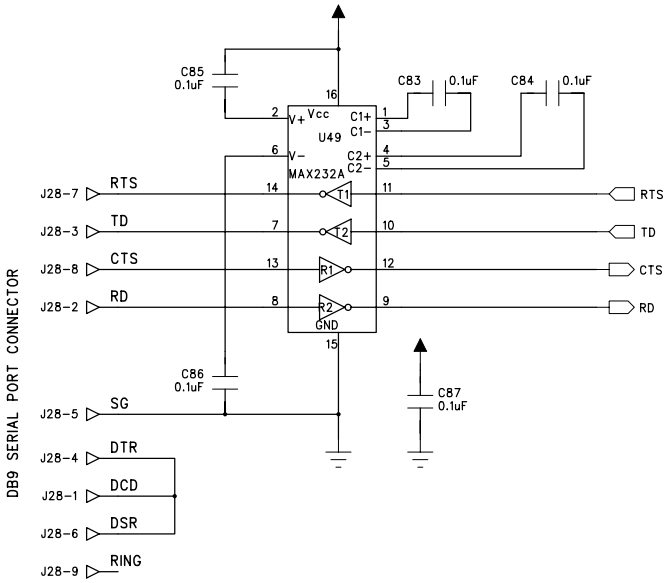


DRAWN:	DATED:
CHECKED:	DATED:
QUALITY CONTROL:	DATED:
RELEASED:	DATED:

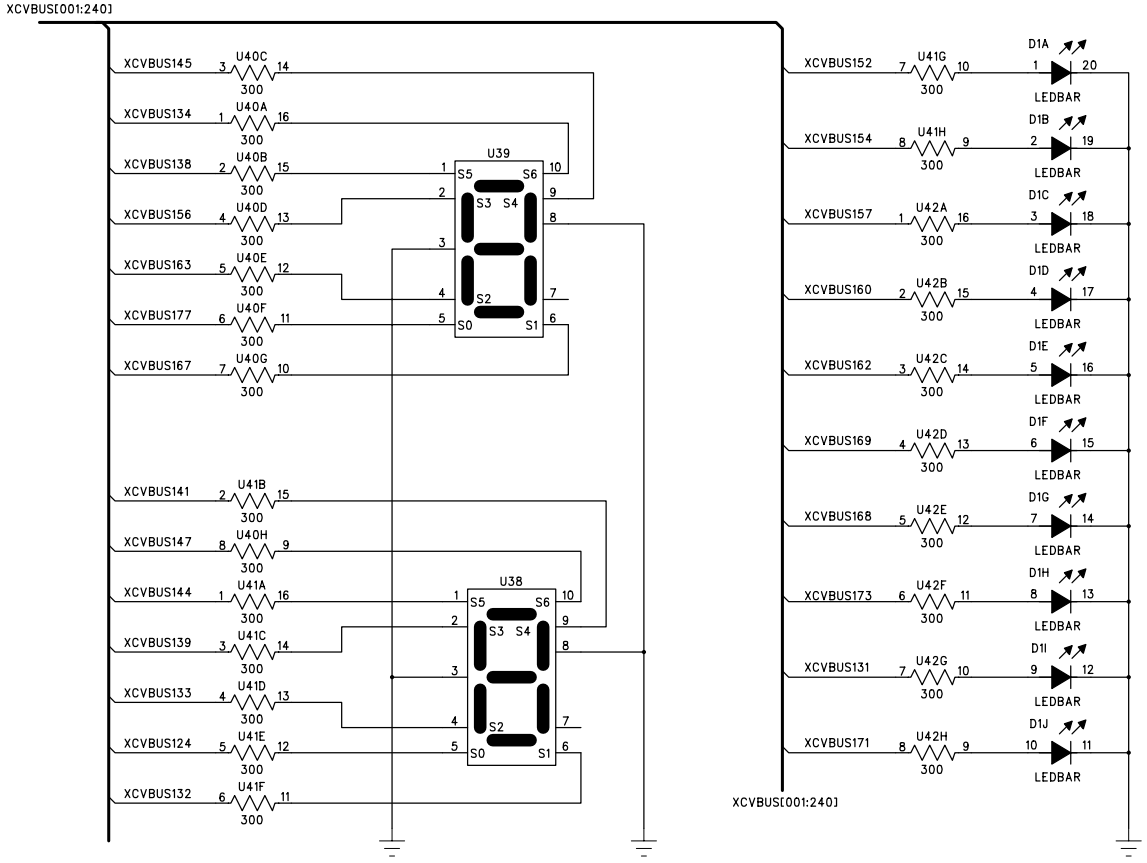
COMPANY: XESS Corp.

TITLE: XSV Board
serial port interface

CODE:	SIZE:	DRAWING NO:	REV:
			1.1

SCALE:

SHEET: 12



REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

DRAWN:	DATED:
CHECKED:	DATED:
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RELEASED:	DATED:

COMPANY: XESS Corp.

TITLE: XSV Board
LED section

CODE:	SIZE:	DRAWING NO:	REV:
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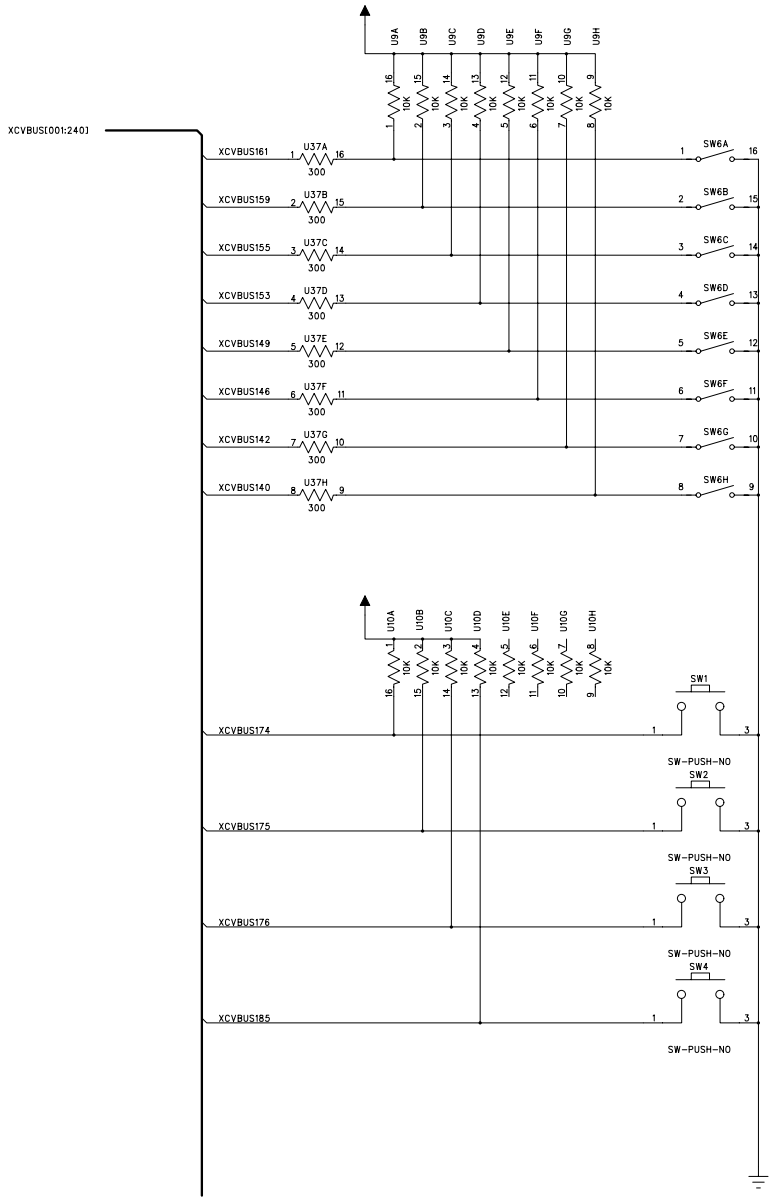
SCALE:

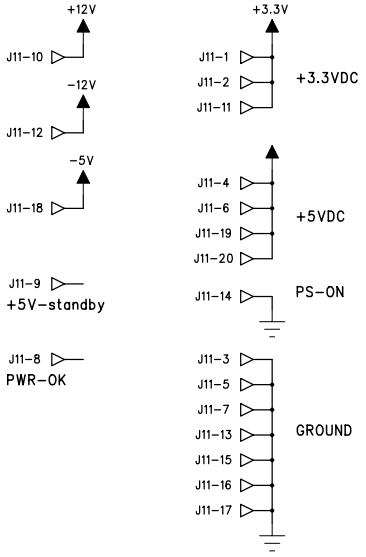
SHEET: 13

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

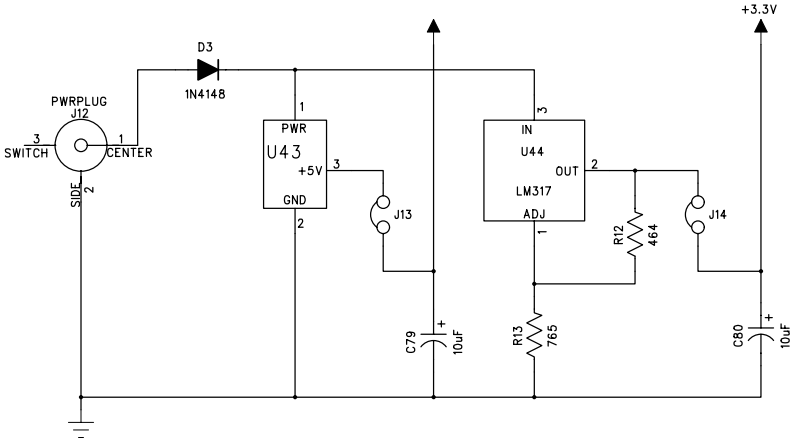


DRAWN:	DATED:	COMPANY: XESS Corp.			
CHECKED:	DATED:	TITLE: XSV Board dip switches and pushbuttons			
QUALITY CONTROL:	DATED:	CODE:	SIZE:	DRAWING NO:	REV: 1.1
RELEASED:	DATED:	SCALE:			SHEET: 14

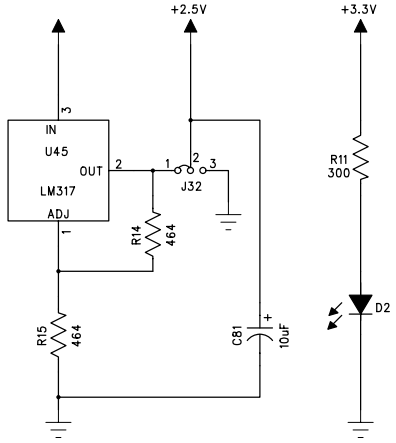
REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

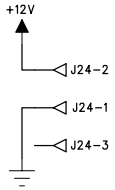


ATX Power Connector



9VDC Power Plug





Cooling Fan Connector

DRAWN:	DATED:
CHECKED:	DATED:
QUALITY CONTROL:	DATED:
RELEASED:	DATED:

COMPANY: XESS Corp.

TITLE: XSV Board
power input & regulation

CODE:	SIZE:	DRAWING NO:	REV:
			1.1

SCALE: | SHEET: 15