FRAME GRABBER PROJECT

Designed in Verilog HDL
&
Implemented on FPGA (XSB 300E board)

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Contents

1.0 About this design

The design is actually an implementation of a frame grabber on FPGA (XSB 300E board) in Verilog HDL. Analog video from an NTSC/PAL camera will be the input signal at the RCA - Jack connector J8 on the XSB 300E board.

The analog signal is digitized by the video decoder (SAA7114) and arrives at the FPGA through the IPD bus. The IPD bus carries the 8-bit luminance values (Y). The data format at the video decoder output is YUV 4:2:2.

A Mealy FSM is used to store a digitized video field on 256K x 16 SRAM .Then this stored field will be displayed on a VGA monitor tuned at 640 x 480 resolution, with the help of a Video DAC THS8133B.

2.0 Files needed for this design

List of Files

- Azhar_fg.v
- xssetsaa.exe
- cfgi2c.bit
- saa7114.txt
- final.ucf
- azhar_fg.bit

File Descriptions

Azhar_fg.v :
The actual behavioral level module that stores field on Sram and tuned the monitor to 640 x 480 resolution and displays the fields in the center of VGA monitor.

xssetsaa.exe:
This file contains an executable program to program the SAA7113 chip through the parallel port. This program was provided by XESS corporation.

cfgi2c.bit :
It programs the I2C bus on SAA7114 video decoder.

saa7114.txt :
It consists of a series of lines with each line having a register address and the value to be loaded into that register. This program was provided by XESS corporation.

final.ucf :
Constraints file for the Frame Grabber design.

azhar_fg.bit
Bit stream file of the design module.

3.0 Description of the design

Using the Frame Grabber project

The frame grabber design does not include the circuitry required to initialize the SAA7114. A utility that will initialize the SAA7114 registers with values from a file on the PC. Once the SAA7114 is initialized, the Frame grabber can be downloaded to the XSB-300E Board whereupon it will begin grabbing and displaying video frames. Splitting the initialization out of the main frame grabber design allows you to easily try different options for the SAA7114 without having to modify the generic frame grabber design.

Here's how to use the frame grabber:

1) Make sure you have XSTOOLS 4.0.3 installed on your PC. Earlier Versions of XSTOOLs do not have support for the XSB-300E Board.

2) Place the xssetsaa.exe and Azhar_fg.bit files into the C:\XSTOOLS folder.

3) Place the cfgi2c.bit and saa7114.txt files into the C:\XSTOOLS\XSB folder.

4) Open a command-line window and go to the C:\XSTOOLS folder.
Then issue the command:
xssetsaa -p 1 -b XSB-300E -f XSB\saa7114.txt

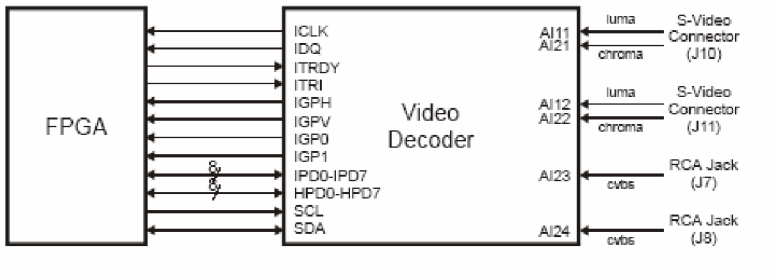
5) Plug a source of NTSC video into RCA jack J8 and a VGA monitor into connector X2 of the XSB-300E Board.

6) Use GXSLOAD to download the fg.bit file into the XSB-300E Board.
The LED2 digit will display a "T" rotated 90 degrees that flashes after every refresh cycle as a new frame of video is grabbed and stored in memory.
The frame of video will be displayed on the VGA monitor.

Specifications

Video Decoder (SAA7114)

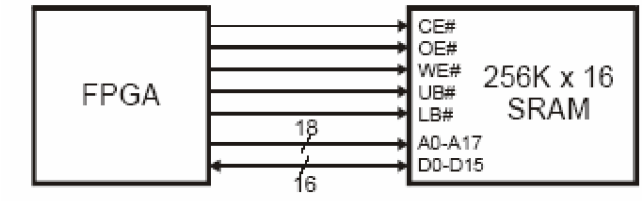
The XSB board can digitize NTSC, SECAM, PAL video signals with this chip. The digitized video arrives at the FPGA over the IPD and HPD buses when IDQ is active .The arrival of video data is synchronized with the ICLK driven from the FPGA.The FPGA can program the I2C bus. Here only IPD bus is used .The ICLK is 27MHZ.



Datasheet available at
http://www-us.semiconductors.philips.com/pip/SAA7114.html

SRAM (TC55V16256FT-15)

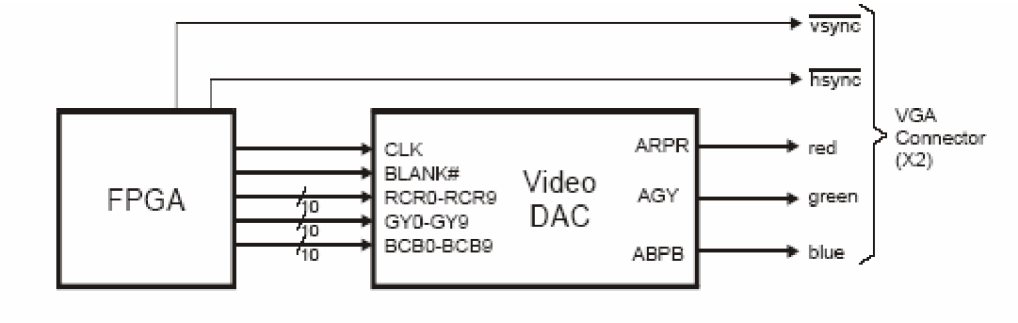
The Frame Grabber project uses the lower byte of SRAM 16 bit data Bus to store the data by concatenating the (18 bit address Bus) row and column addresses of the pixel. Each address stores the data for a 8 bit pixel. The row address is the upper 8 bits of the address used. And column address is lower 10 bits of the address used.



Datasheet available at
http://www.toshiba.com/taec/components/Datasheet/55v16256.pdf

DISPLAY

The VGA monitor is tuned at 640 x 480 pixels. For PAL standard the frame is of 240 x 361 pixels displayed at the center of monitor. Hsync, Vsync and blank signals are generated for the video DAC (THS8133B) and CLk is 27MHZ.



Datasheet available at
http://focus.ti.com/lit/ds/symlink/ths8133b.pdf

Extensions

There are many extensions that could be done to this project to increase the use of the project .More detailed document will be updated soon!

References

http://www.xess.com
http://focus.ti.com/lit/ds/symlink/ths8133b.pdf
http://www.toshiba.com/taec/components/Datasheet/55v16256.pdf
http://www-us.semiconductors.philips.com/pip/SAA7114.html
http://www.xilinx.com/