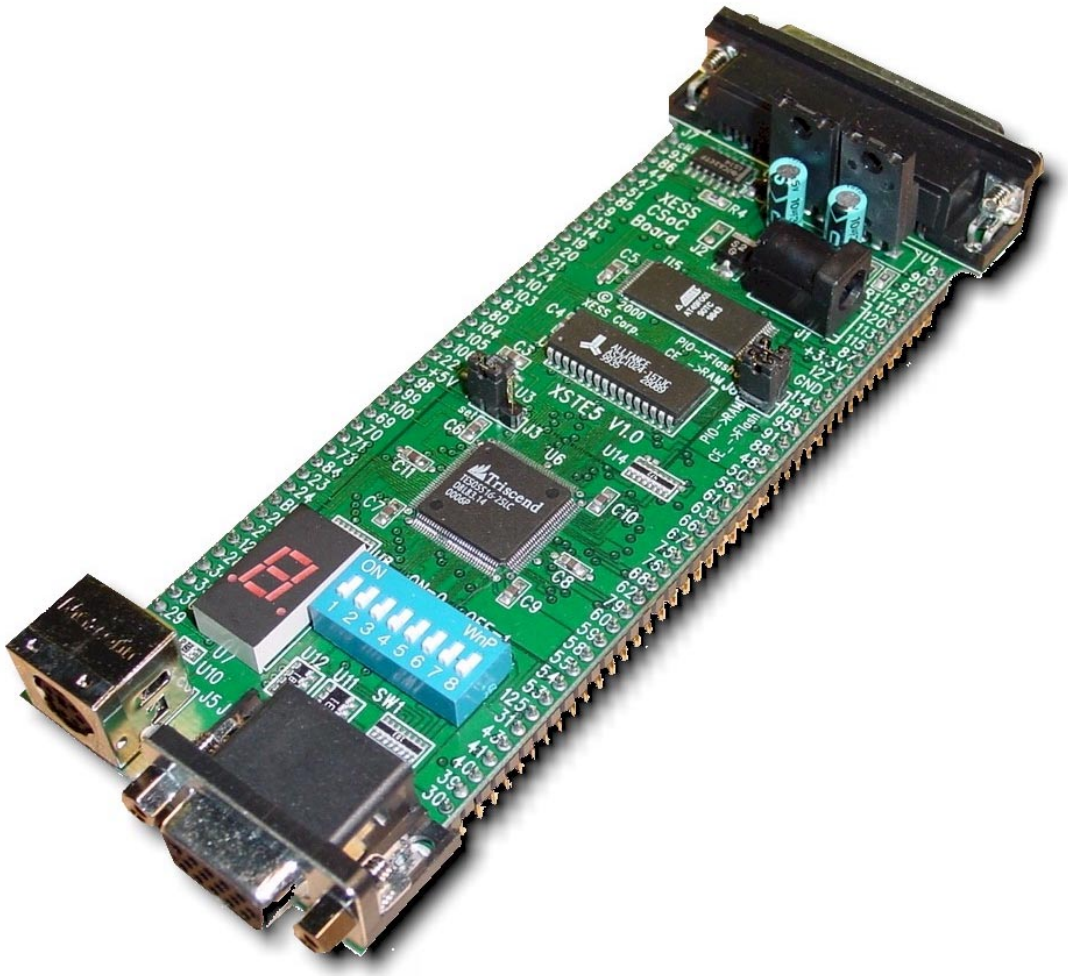
myCSoC

CSoC Board Manual



Version 1.0
6/13/00

XESS Corporation

XSTE5 CSoC Board Manual

Take Notice!!

- The XSTE5 CSoC Board requires an external power supply to operate! It does not draw power through the downloading cable from the PC parallel port.
- If you are connecting a 9VDC power supply to your CSoC Board, please make sure the center terminal of the plug is positive and the outer sleeve is negative.
- The CSoC Board uses a programmable oscillator with a default frequency of 50 MHz. You must reprogram the oscillator if you want to use another frequency. The procedure for doing this is described on page 6.

XSTE5 CSoC Board Components

The XSTE5 CSoC Board is shown in Figure 1. It contains the following components:

Triscend TE505 CSoC: The TE505 contains an enhanced 8032 microcontroller, two DMA controllers, 16 KBytes of internal SRAM, and an array of 512 programmable logic cells.

128 KByte SRAM: The 15ns SRAM can be used for general-purpose data storage or it can hold instructions and data for the microcontroller in the CSoC.

128 KByte Flash RAM: The Flash RAM can store the configuration and programs for the CSoC and restore them after a power interruption.

100 MHz Programmable Oscillator: A nonvolatile programmable divider in this oscillator chip lets it output a clock in the frequency range of 50 KHz to 100 MHz to the rest of the CSoC Board.

Seven-Segment LED: The CSoC can show simple status indicators through this display device:

DIP Switch: The CSoC can receive up to eight logic inputs from this bank of switches.

Parallel Port: CSoC configurations are downloaded and debugged on the CSoC Board using a PC connected to the parallel port connector.

PS/2 Port: The CSoC can receive data from a standard keyboard or mouse through this connector.

VGA Port: The CSoC can generate video signals for a VGA monitor attached to this connector.

Prototyping Interface: The majority of the I/O pins of the CSoC are made available to external devices through this set of 84 pins on the underside of the CSoC Board.

Power Jack: A 9V DC input to this jack is converted into the +3.3V and +5V supplies required by the rest of the CSoC Board circuitry.

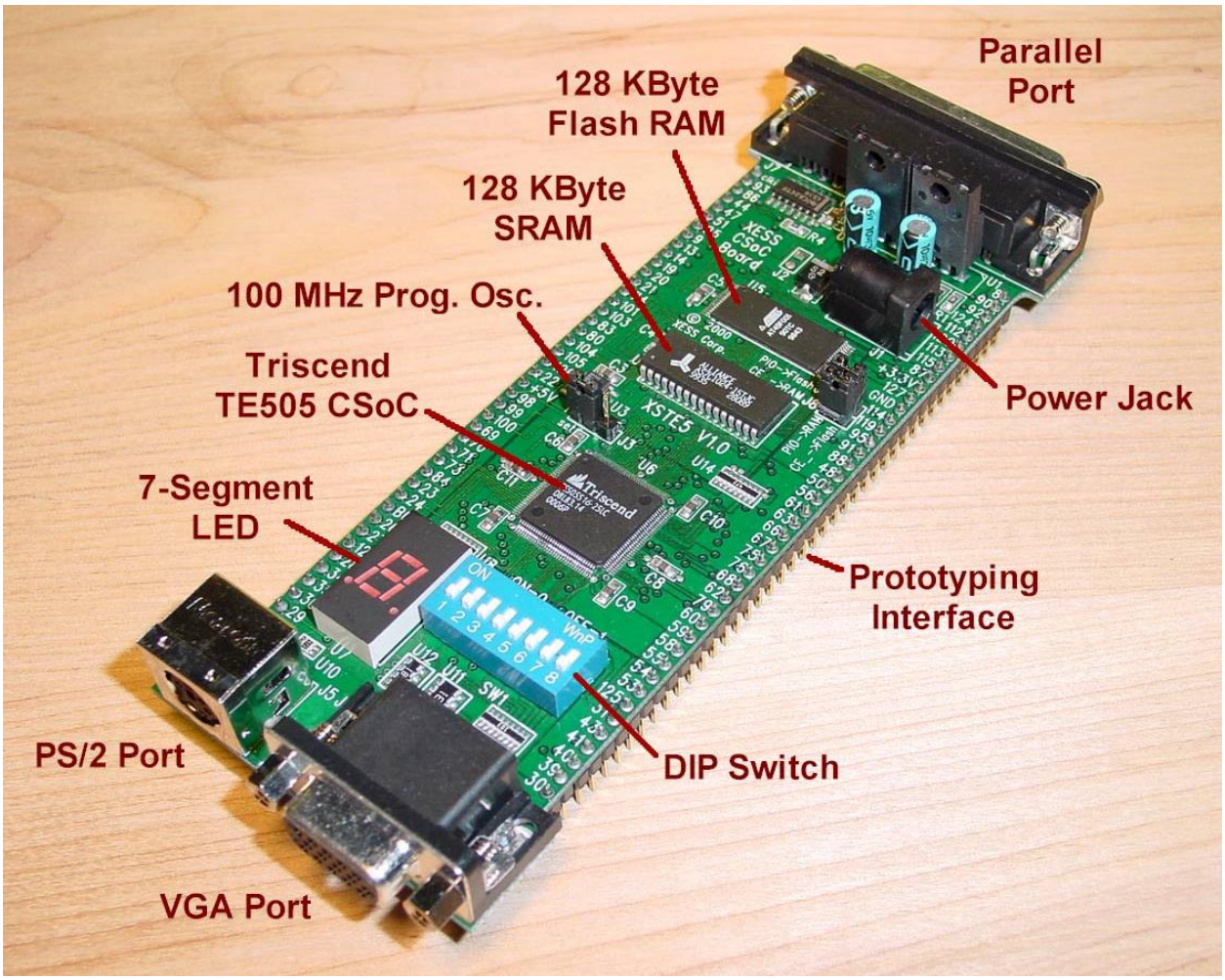


Figure 1: XSTE5 CSoC Board.

Applying Power to Your CSoC Board

You can use your CSoC Board in two ways, distinguished by the method you use to apply power to the board.

Using a 9VDC wall-mount

You can use your CSoC Board all by itself to experiment with logic and microcontroller designs. Just place the CSoC Board on a non-conducting surface as shown in Figure 2. Then apply power to jack J1 of the board from a 9V DC, 500 mA wall-mount transformer with a 2.1 mm female, center-positive plug. The on-board regulators will convert the 9V into the +3.3V and +5V supplies required by the rest of the CSoC Board circuitry.

Solderless Breadboard Installation

The two rows of pins from your CSoC Board can be plugged into a solderless breadboard with holes spaced at 0.1" intervals. (One of the A.C.E. protoboards from 3M is a good choice.) Once plugged in, all the pins of the Triscend CSoC, SRAM, and Flash RAM are accessible to other circuits on the breadboard. (The numbers printed next to the rows of pins on your CSoC Board correspond to the pin numbers of the Triscend CSoC.) Power can still be supplied to your CSoC Board though jack J1, or power can be applied directly through several pins on the underside of the board. Just connect +5V, +3.3V, and ground from an external power supply to the pins with those labels.

Connecting a PC to Your CSoC Board

The 6' downloading cable included with your CSoC Board connects it to a PC. One end of the cable attaches to the parallel port on the PC and the other connects to the female DB-25 connector (J7) at the top of your CSoC Board as shown in Figure 2.

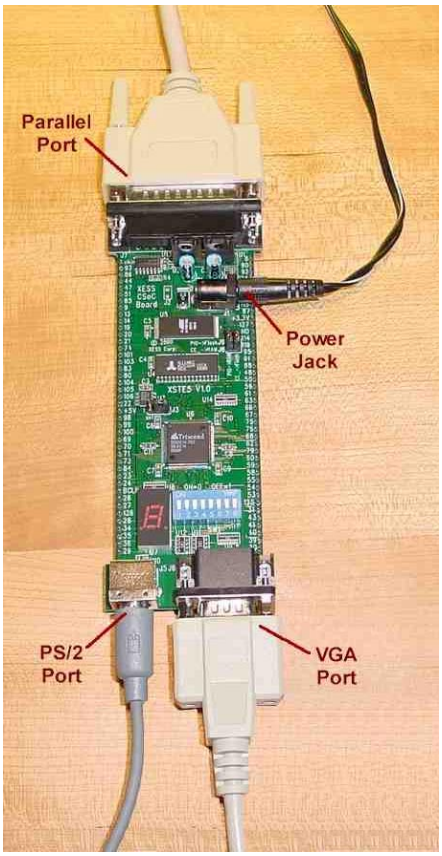


Figure 2: Connections from the XSTE5 CSoC Board to external devices.

Connecting a VGA Monitor to Your CSoC Board

You can display images on a VGA monitor by connecting it to the VGA port (connector J6) at the bottom of your CSoC Board (see Figure 2). You will have to download a VGA driver circuit to your CSoC Board to actually display an image.

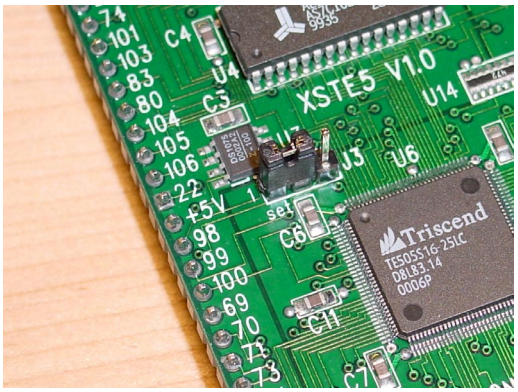
Connecting a Mouse or Keyboard to Your CSoC Board

You can accept inputs from a keyboard or mouse by connecting it to the PS/2 port (connector J5) at the bottom of your CSoC Board (see Figure 2).

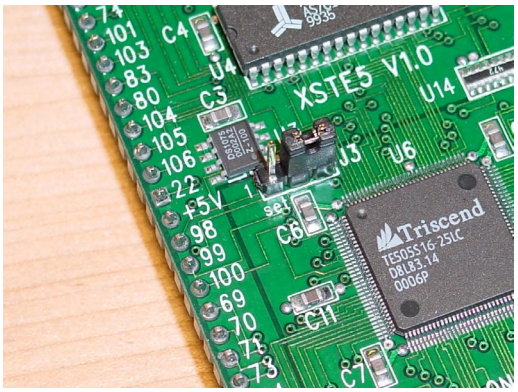
Setting the Jumpers on Your CSoC Board

The CSoC Board contains two sets of jumpers: one jumper that controls the mode of the programmable oscillator, and a dual-jumper that selects which memory device holds the program instructions and data for the CSoC.

The programmable oscillator is controlled by jumper J3. The position of the shunt on J3 determines the oscillator mode when power is applied to the CSoC Board. You should disconnect the power supply from jack J1 and the downloading cable from parallel port J7 before moving the shunt on J3. Otherwise the programmable oscillator will ignore the shunt setting. The oscillator will respond to the shunt setting when power is restored to the CSoC Board. The two shunt settings for J3 are discussed below.

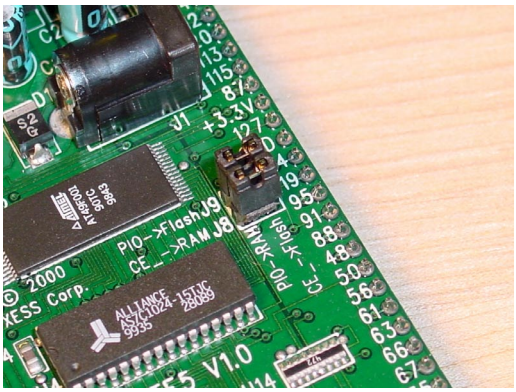


The shunt on jumper J3 should be in the "set" position if you want to program the frequency of the oscillator on the CSoC Board. Then you can use a software utility to set the programmable frequency divider in the oscillator. The divisor value is stored in Flash within the oscillator chip so it will not be cleared if power is removed from the CSoC Board.

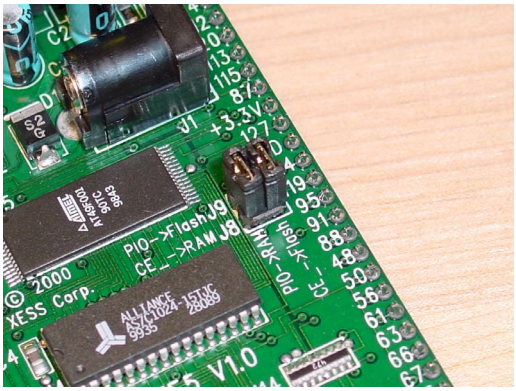


The shunt on jumper J3 should be in the "osc" position when you want the oscillator to output a clock signal to the CSoC. The programmable oscillator will divide its internal 100 MHz frequency source by the divisor value stored in Flash. This is the default position for the shunt.

The connection of the SRAM and Flash RAM memory chips to the CSoC is controlled by jumpers J8 and J9. The orientation of the shunts on J8 and J9 will attach the chip-enable of one of the memory devices to the dedicated chip-enable output of the CSoC. Then the CSoC will fetch instructions and data from this memory device. The chip-enable of the other memory device will be connected to a general-purpose I/O pin of the CSoC. The CSoC can still access this memory chip but it requires some extra programming effort on your part to do so. The two possible shunt settings for J8 and J9 are shown below.



The CSoC will get instructions and data from the 128 KByte SRAM when the shunts are oriented horizontally on jumpers J8 and J9. This is the default shunt setting and should be used when you are developing a CSoC design because downloading into the SRAM is much faster than programming the Flash RAM.



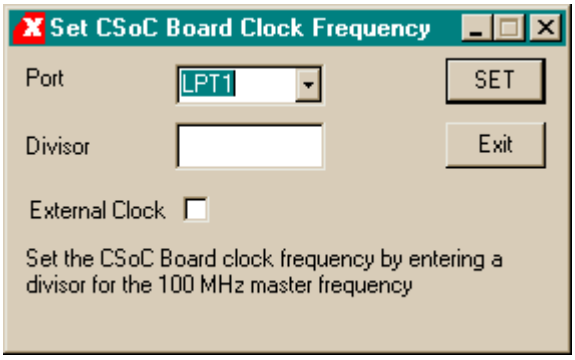
The CSoC will get instructions and data from the 128 KByte Flash RAM when the shunts are oriented vertically on jumpers J8 and J9. This is the setting to use when your CSoC design is finalized and you want to store it in the Flash RAM. Then the CSoC will initialize itself from the Flash whenever power is applied to the CSoC Board.

Programming the Oscillator Frequency

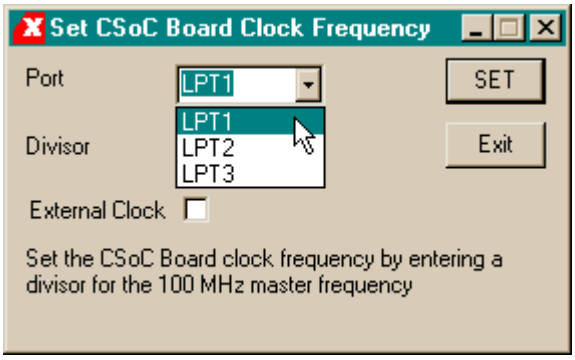
Before programming your CSoC Board, you need to set the programmable oscillator to a frequency that is compatible with the Triscend TE505 CSoC. The CSoC on your board has a maximum operating frequency of 25 MHz so the oscillator output clock can't be any higher than that.

Click on the 

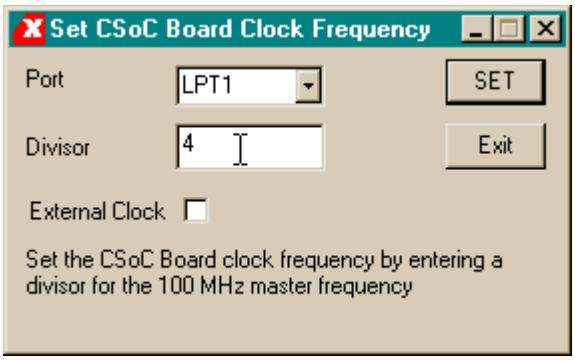
icon to begin the oscillator programming process. The window shown below will appear.



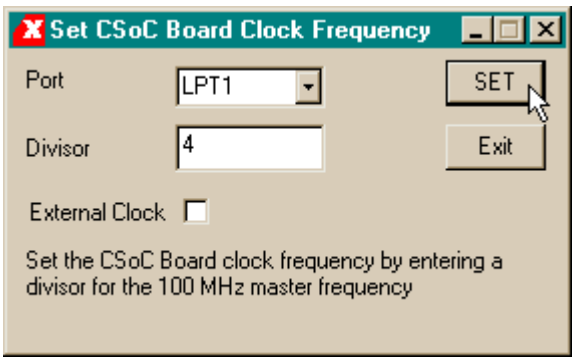
Select the PC parallel port that is connected to your CSoC Board from the drop-down menu as shown below. In the majority of cases, this will be LPT1.



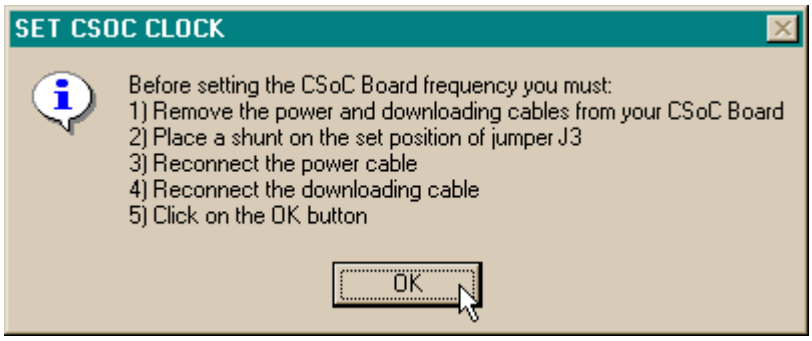
Next, type in the divisor for the 100 MHz master frequency. Allowable divisors are in the range [1,2052]. If you want to run the CSoC at its maximum speed of 25 MHz, enter `4` into the Divisor box.



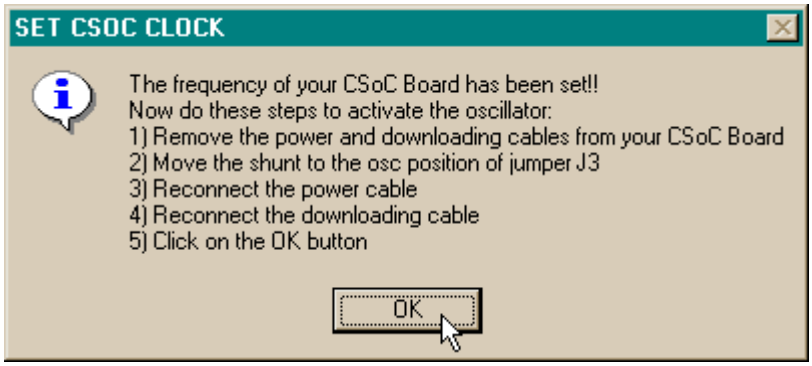
Then click on SET to begin sending the programming commands to the oscillator chip.



The program will provide you with a list of steps to perform that will place the oscillator chip in the programming mode. Once you have done these steps in the given sequence, click on OK.



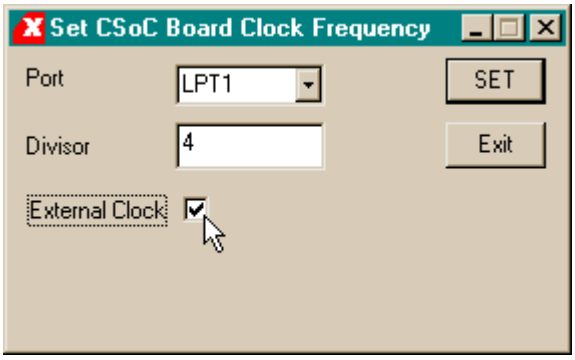
The program will load the divisor into the oscillator chip very quickly. Then it will give you a list of steps to do that will end the oscillator programming mode and cause it to output the frequency you specified. Once you have done these steps in the given sequence, click on OK.



At this point, the programmable oscillator should be generating a clock for the CSoC derived from its internal 100 MHz frequency source.

If you wish to use an external clock to drive the CSoC Board instead of the 100 MHz oscillator, just click on the External Clock checkbox and repeat the steps listed above. Then attach your external clock to the clkin pin in the upper left-hand corner of your CSoC Board. The external clock will be divided by the divisor in the programmable

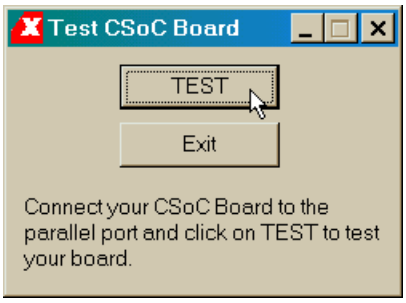
oscillator and then passed to the CSoC. The maximum allowable external clock frequency is 50 MHz.



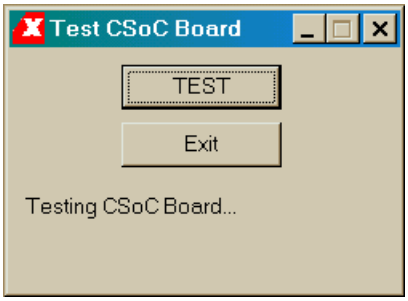
Testing Your CSoC Board

You can check the health of your CSoC Board by clicking on the 

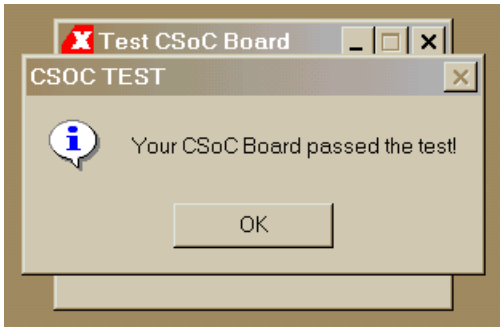
icon. Press on the TEST button in the **Test CSoC Board** window.



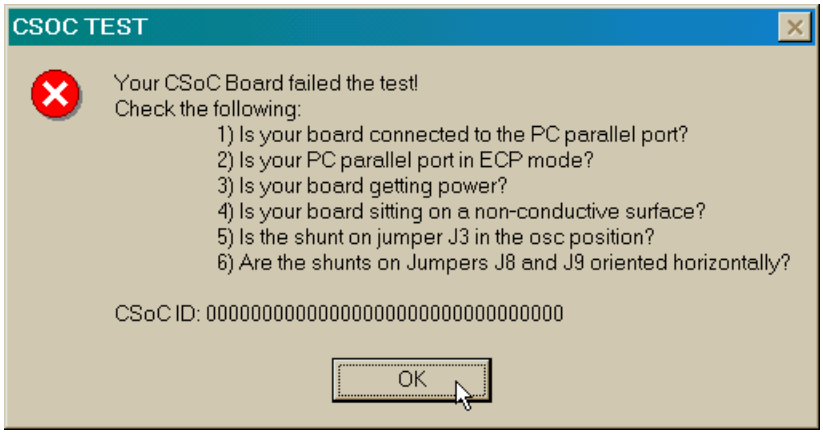
The LED segments on your CSoC Board will light in sequence and the **Test CSoC Board** window will indicate that the board test is in progress.



If your CSoC Board passes the test, you will see a `0` displayed on the seven-segment LED and the following window will appear. You can now proceed with designing CSoC-based systems using your CSoC Board.



If your CSoC Board fails the test, you will see a window that gives you several items to check that may have caused the failure.



If all these checks are positive, then test the board using another PC. In our experience, 99.9% of all problems are due to the parallel port. If you cannot get your CSoC Board to pass the test, then contact XESS Corp. at help@xess.com.

CSoC Board Circuitry

A high-level view of the CSoC Board circuitry is shown in Figure 3.

The eight data pins from the PC parallel port terminate on the CSoC. D0 controls the CSoC reset pin and is normally not connected (jumper J2 is left open). D1 and D2 attach to the TMS and TCK pins that control the JTAG state machine in the CSoC. Configuration and debugging commands are sent to the TDI input of the CSoC JTAG port over D3. The upper nybble of the parallel port data bits (D4–D7) is available as general-purpose inputs to the CSoC from the PC as are the four control outputs from the parallel port (C0–C3). Control bit C2 passes through two Schmitt-trigger inverters before reaching one of the global buffer inputs (GBUF5) of the CSoC, so this bit can be

used to pass a low-speed clock from the PC. The other data and control bits have slow edge transition times and are not suitable for use as clocks unless you use the Schmitt-trigger option on the CSoC input pins.

The CSoC can communicate back to the PC through the parallel port status inputs S3–S7. The most-significant status bit (S7) is used by the TDO pin of the CSoC JTAG port to pass debugging information back to the PC. The remaining status bits are available as general-purpose outputs from the CSoC back to the PC.

A DIP switch with eight individual SPST switches is attached to the CSoC. A switch is open when it is in the OFF position and the corresponding pin of the CSoC is pulled to the supply voltage through a pull-up resistor. When the switch is ON (closed), it pulls the CSoC pin directly to ground.

The CSoC receives data from a keyboard or mouse through the two inputs connected to the PS/2 port. The data input delivers a serial data stream which is accepted into the CSoC on the falling edges of the clock input.

Seven outputs from the CSoC drive a seven-segment LED digit. These same outputs also drive the inputs to a VGA monitor. Horizontal and vertical sync outputs from the CSoC generate a stable timing reference for the frames of video sent to the monitor. The other six outputs determine the color of the current pixel in the video frame. Sixty-four pixel colors are possible (4 levels of red $\times$ 4 levels of green $\times$ 4 levels of blue).

The programmable oscillator output goes directly to the input of the CSoC.

The CSoC can write and read data to and from a 128 KByte SRAM and a 128 KByte Flash RAM on the CSoC Board. The SRAM and Flash RAM interface to the CSoC through a 17-bit address bus and an 8-bit data bus. Active-low chip-enable, output-enable, and write-enable control lines to the SRAM and Flash RAM are driven by the CSoC to activate the devices and either read or write a byte of data. The connection of the SRAM and Flash RAM memory chips to the CSoC is controlled by jumpers J8 and J9. The orientation of the shunts on J8 and J9 will attach the chip-enable of one of the memory devices to the dedicated chip-enable output of the CSoC. Then the CSoC will fetch instructions and data from this memory device. The chip-enable of the other memory device will be connected to a general-purpose I/O pin of the CSoC. The CSoC can still access this memory chip but it requires some extra programming effort on your part to do so.

The remaining pins of the CSoC are not committed to any specific function. They can be used as general-purpose I/O. Four of these pins also serve as inputs to global buffers in the CSoC so they are suitable as clock inputs to circuitry housed in the CSL of the CSoC. Two of the uncommitted pins (VSYS and SLAVE) control the startup and operating mode of the CSoC and you shouldn't use them unless you know what you are doing.

All the pins in Figure 3 that are tagged with a small rectangle are accessible to external systems through the pins which exit the bottom of the CSoC Board. The pins on the CSoC Board are labeled with the pin number of the CSoC pin to which they attach.

Condensed and expanded lists of the CSoC Board pins and their connections are given in Table 1 and Table 2, respectively. The detailed CSoC Board schematics follow these tables.

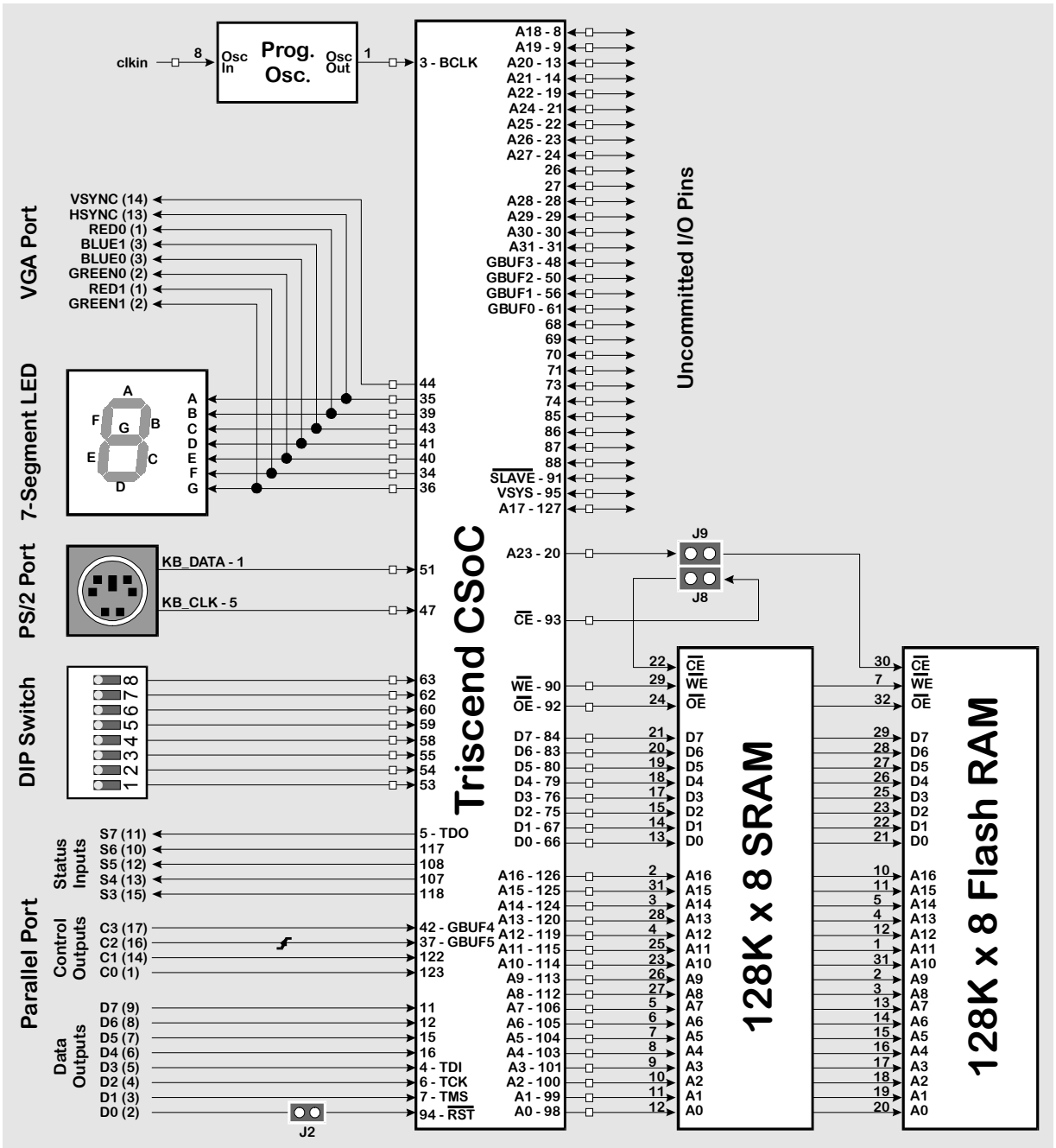


Figure 3: CSoC Board high-level schematic.

Table 1: Connections between the TE505 and other CSoC Board components.

TE505		CSoC Board	
Pin	Name	Function	Pin
1	GND		
2	XTALIN		
3	XTALOUT		64,13
4	TDI	PPORT D3 (5)	
5	TDO	PPORT S7 (11)**	
6	TCK	PPORT D2 (4)**	
7	TMS	PPORT D1 (3)	
8	A18		63
9	A19		71
10	GND		
11	PIO_0	PPORT D7 (9)	
12	PIO_1	PPORT D6 (8)	
13	A20		72
14	A21		73
15	PIO_2	PPORT D5 (7)	
16	PIO_3	PPORT D4 (6)	
17	VCC		2*
18	GND		
19	A22		74
20	A23	RAM/Flash /CE	75
21	A24		76
22	A25		1
23	A26		11
24	A27		12
25	GND		
26	PIO_8		14
27	PIO_9		15
28	A28		17
29	A29		21
30	A30		22
31	A31		27
32	VCC		

TE505		CSoC Board	
Pin	Name	Function	Pin
33	GND		
34	PIO_18	Red1,SegF	18
35	PIO_19	HSync,SegA	19
36	PIO_20	Green1,SegG	20
37	GBUF5	PPORT C2 (16)**	
38	GND		
39	PIO_21	Red0,SegB	23
40	PIO_22	Green0,SegE	24
41	PIO_23	Blue0,SegD	25
42	GBUF4	PPORT C3 (17)	
43	PIO_24	Blue1,SegC	26
44	PIO_25	Vsync	67
45	CVCC**		
46	CGND**		
47	PIO_26	PS/2 Clk	68
48	GBUF3		46
49	GND		
50	GBUF2		45
51	PIO_27	PS/2 Data	69
52	VCC		
53	PIO_28	Switch1	29
54	PIO_29	Switch2	30
55	PIO_30	Switch3	31
56	GBUF1		44
57	GND		
58	PIO_31	Switch4	32
59	PIO_32	Switch5	33
60	PIO_35	Switch6	34
61	GBUF0		43
62	PIO_38	Switch7	36
63	PIO_39	Switch8	42
64	VCC		

TE505		CSoC Board	
Pin	Name	Function	Pin
65	GND		
66	D0	RAM/Flash D0	41
67	D1	RAM/Flash D1	40
68	PIO_52		37
69	PIO_53		6
70	PIO_54		7
71	PIO_55		8
72	GND		
73	PIO_60		9
74	PIO_61		77
75	D2	RAM/Flash D2	39
76	D3	RAM/Flash D3	38
77	CVCC		
78	CGND		
79	D4	RAM/Flash D4	35
80	D5	RAM/Flash D5	81
81	VCC		
82	GND		
83	D6	RAM/Flash D6	80
84	D7	RAM/Flash D7	10
85	PIO_62		70
86	PIO_63		66
87	PIO_64		55
88	XDONE		47
89	GND		52
90	WE_	RAM/Flash /WE	62
91	SLAVE		48
92	OE_	RAM/Flash /OE	61
93	CE_	RAM/Flash /CE	65
94	RST_	PPORT D0 (2)	
95	VSYS		49
96	VCC		54

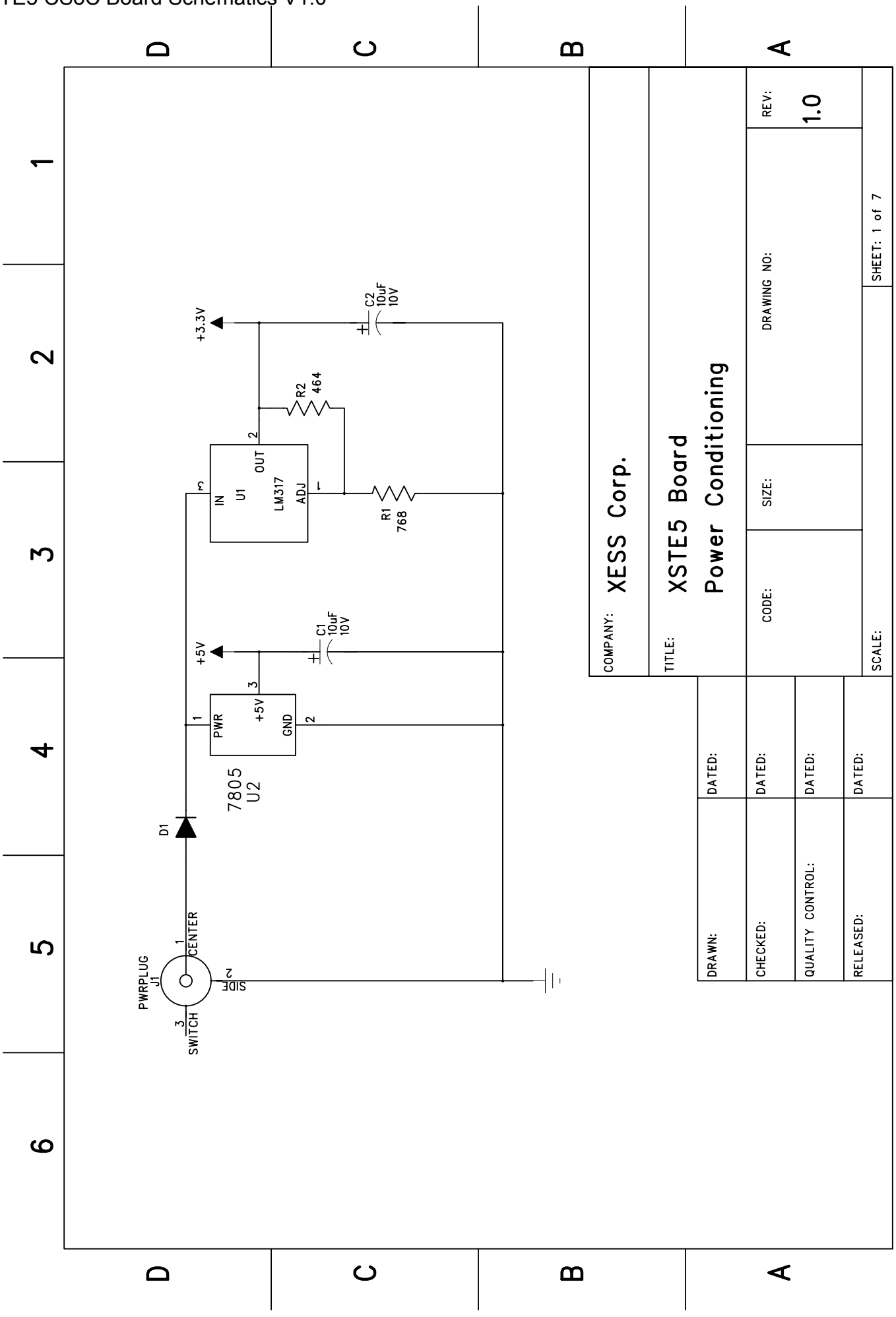
TE505		CSoC Boa
Pin	Name	Function
97	GND	
98	A0	RAM/Flash A0
99	A1	RAM/Flash A1
100	A2	RAM/Flash A2
101	A3	RAM/Flash A3
102	GND	
103	A4	RAM/Flash A4
104	A5	RAM/Flash A5
105	A6	RAM/Flash A6
106	A7	RAM/Flash A7
107	PIO_65	PPORT S4 (13)
108	PIO_66	PPORT S5 (12)
109	GND	
110	CVCC**	
111	CGND**	
112	A8	RAM/Flash A8
113	A9	RAM/Flash A9
114	A10	RAM/Flash A10
115	A11	RAM/Flash A11
116	VCC	
117	PIO_67	PPORT S6 (10)
118	PIO_68	PPORT S3 (15)
119	A12	RAM/Flash A12
120	A13	RAM/Flash A13
121	GND	
122	PIO_69	PPORT C1 (14)
123	PIO_70	PPORT C0 (1)
124	A14	RAM/Flash A14
125	A15	RAM/Flash A15
126	A16	RAM/Flash A16
127	A17	Flash A17
128	VCC	

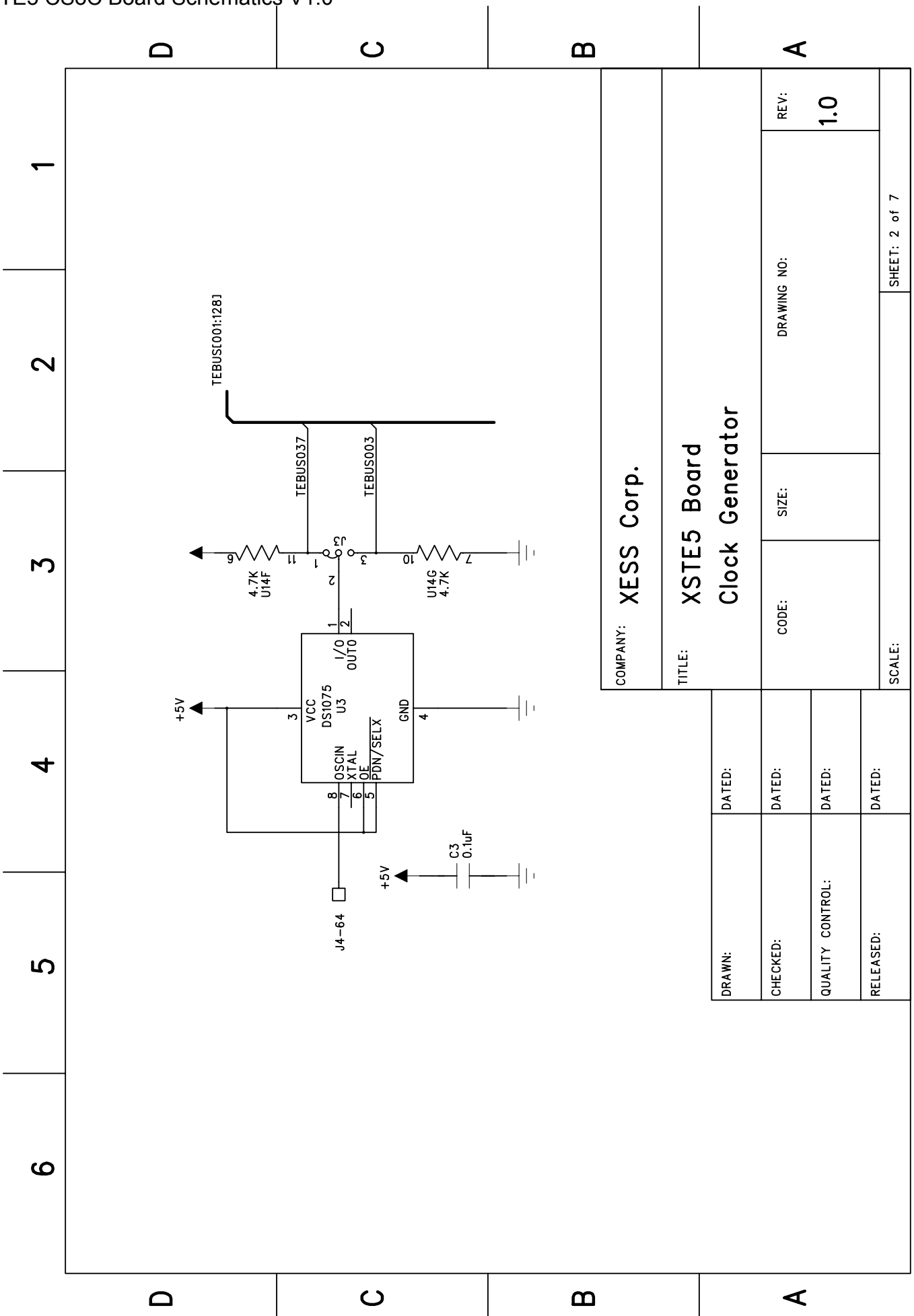
Table 2: Connections between the TE505 and other CSoC Board components. (Expanded version.)

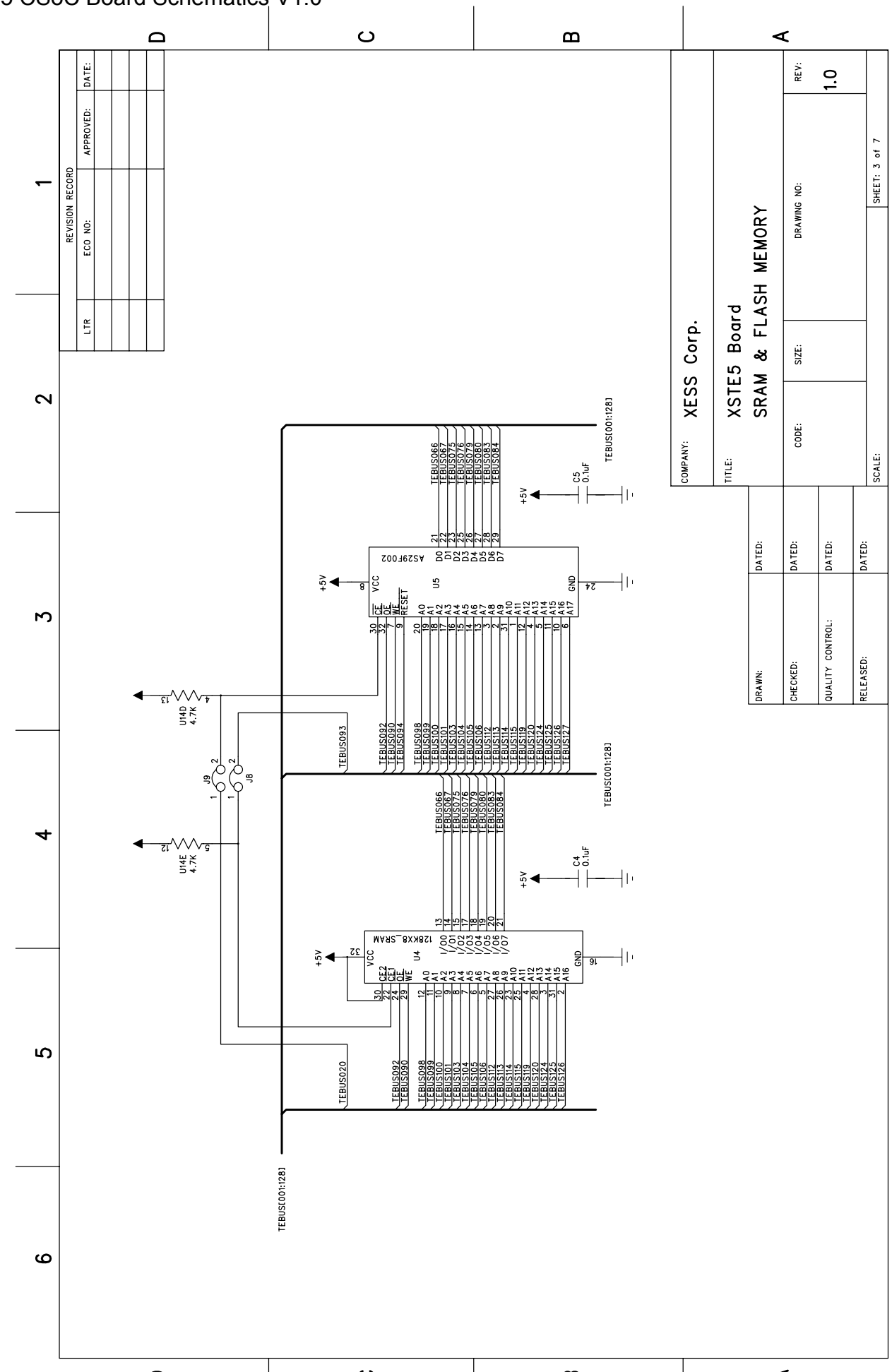
TE505		Pins	Parallel Port	VGA	PS/2	Switches	LEDs	Flash RAM	SRAM	Prog. Osc.
1	GND									
2	XTALIN									
3	XTALOUT	13								Osc Out
4	TDI		D3 (5)							
5	TDO		S7 (11)**							
6	TCK		D2 (4)**							
7	TMS		D1 (3)							
8	A18	63								
9	A19	71								
10	GND									
11	PIO_0		D7 (9)							
12	PIO_1		D6 (8)							
13	A20	72								
14	A21	73								
15	PIO_2		D5 (7)							
16	PIO_3		D4 (6)							
17	VCC	2*								
18	GND									
19	A22	74								
20	A23	75						/CE-PIO	/CE-PIO	
21	A24	76								
22	A25	1								
23	A26	11								
24	A27	12								
25	GND									
26	PIO_8	14								
27	PIO_9	15								
28	A28	17								
29	A29	21								
30	A30	22								
31	A31	27								
32	VCC									
33	GND									
34	PIO_18	18		Red1			SegF			
35	PIO_19	19		Hsync			SegA			
36	PIO_20	20		Green1			SegG			
37	GBUF5		C2 (16)**							
38	GND									
39	PIO_21	23		Red0			SegB			
40	PIO_22	24		Green0			SegE			
41	PIO_23	25		Blue0			SegD			
42	GBUF4		C3 (17)							
43	PIO_24	26		Blue1			SegC			
44	PIO_25	67		Vsync						
45	CVCC**									
46	CGND**									
47	PIO_26	68			Clk					

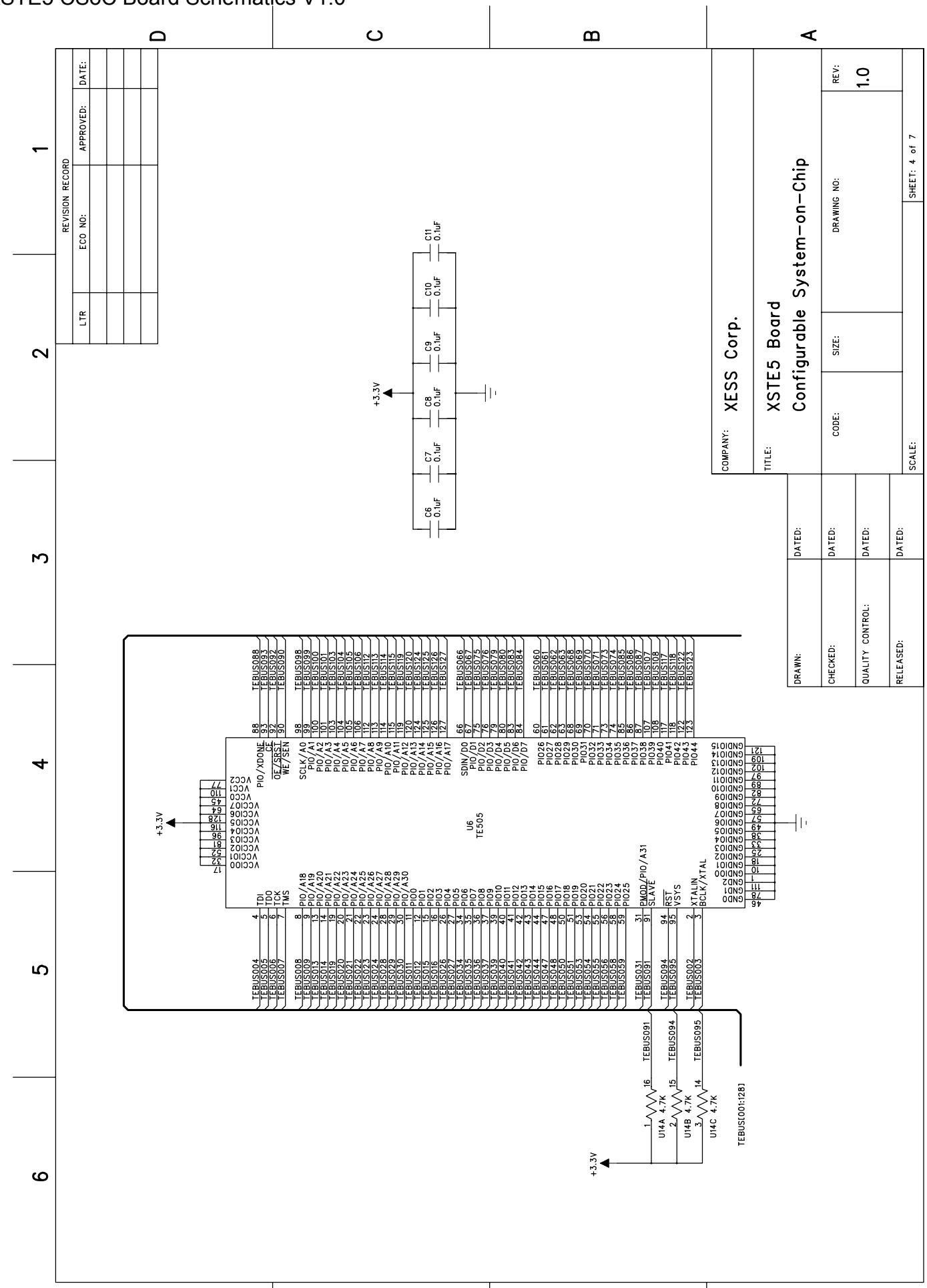
TE505		Pins	Parallel Port	VGA	PS/2	Switches	LEDs	Flash RAM	SRAM	Prog. Osc.
48	GBUF3	46								
49	GND									
50	GBUF2	45								
51	PIO_27	69			Data					
52	VCC									
53	PIO_28	29				Switch1				
54	PIO_29	30				Switch2				
55	PIO_30	31				Switch3				
56	GBUF1	44								
57	GND									
58	PIO_31	32				Switch4				
59	PIO_32	33				Switch5				
60	PIO_35	34				Switch6				
61	GBUF0	43								
62	PIO_38	36				Switch7				
63	PIO_39	42				Switch8				
64	VCC									
65	GND									
66	D0	41						D0	D0	
67	D1	40						D1	D1	
68	PIO_52	37								
69	PIO_53	6								
70	PIO_54	7								
71	PIO_55	8								
72	GND									
73	PIO_60	9								
74	PIO_61	77								
75	D2	39						D2	D2	
76	D3	38						D3	D3	
77	CVCC									
78	CGND									
79	D4	35						D4	D4	
80	D5	81						D5	D5	
81	VCC									
82	GND									
83	D6	80						D6	D6	
84	D7	10						D7	D7	
85	PIO_62	70								
86	PIO_63	66								
87	PIO_64	55								
88	XDONE	47								
89	GND	52								
90	WE_	62						/WE	/WE	
91	SLAVE	48								
92	OE_	61						/OE	/OE	
93	CE_	65						/CE	/CE	
94	RST_		D0 (2)							
95	VSYS	49								
96	VCC	54								
97	GND									
98	A0	3						A0	A0	

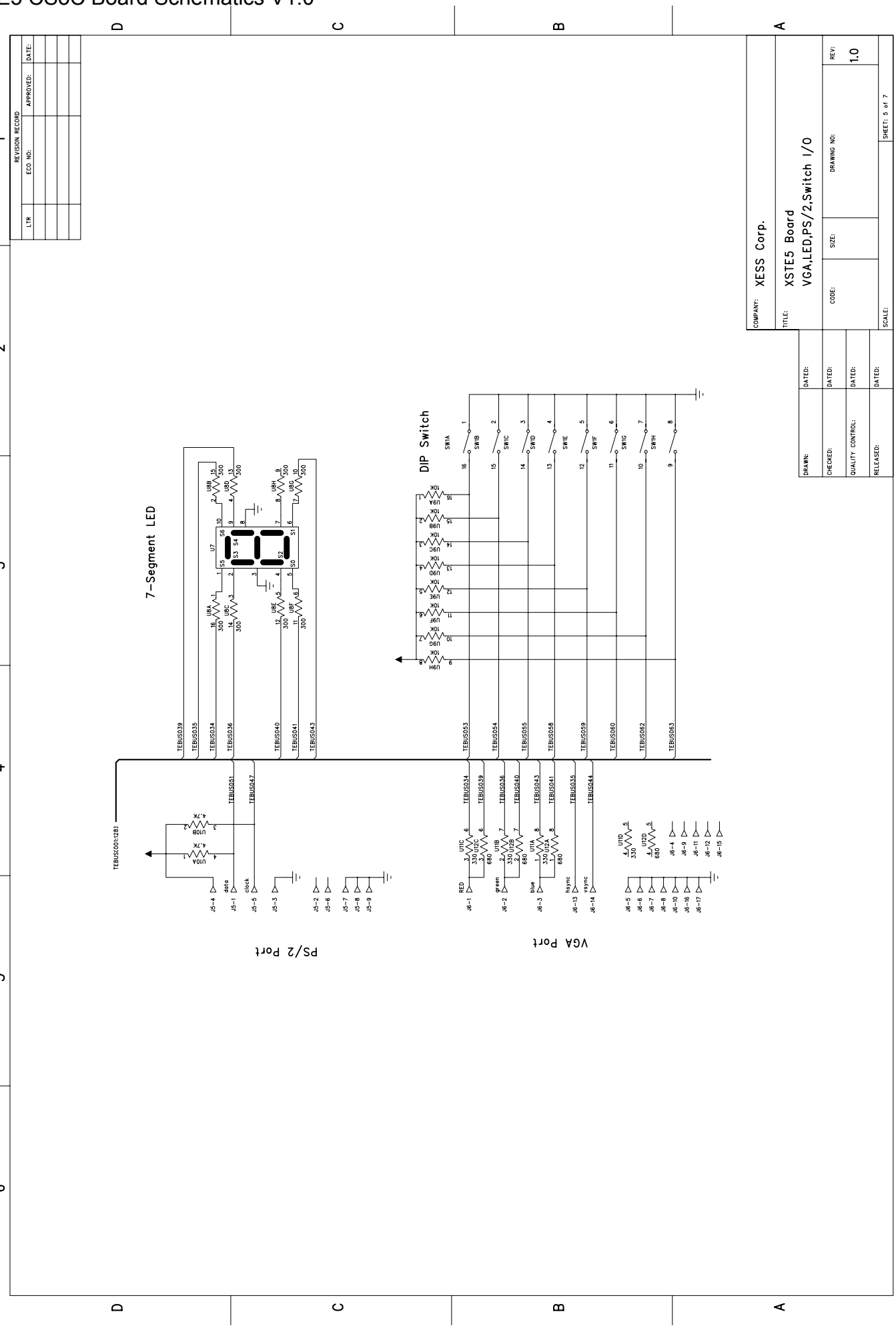
TE505		Pins	Parallel Port	VGA	PS/2	Switches	LEDs	Flash RAM	SRAM	Prog. Osc.
99	A1	4						A1	A1	
100	A2	5						A2	A2	
101	A3	78						A3	A3	
102	GND									
103	A4	79						A4	A4	
104	A5	82						A5	A5	
105	A6	83						A6	A6	
106	A7	84						A7	A7	
107	PIO_65		S4 (13)							
108	PIO_66		S5 (12)							
109	GND									
110	CVCC**									
111	CGND**									
112	A8	59						A8	A8	
113	A9	57						A9	A9	
114	A10	51						A10	A10	
115	A11	56						A11	A11	
116	VCC									
117	PIO_67		S6 (10)							
118	PIO_68		S3 (15)							
119	A12	50						A12	A12	
120	A13	58						A13	A13	
121	GND									
122	PIO_69		C1 (14)							
123	PIO_70		C0 (1)							
124	A14	60						A14	A14	
125	A15	28						A15	A15	
126	A16	16						A16	A16	
127	A17	53						A17		
128	VCC									

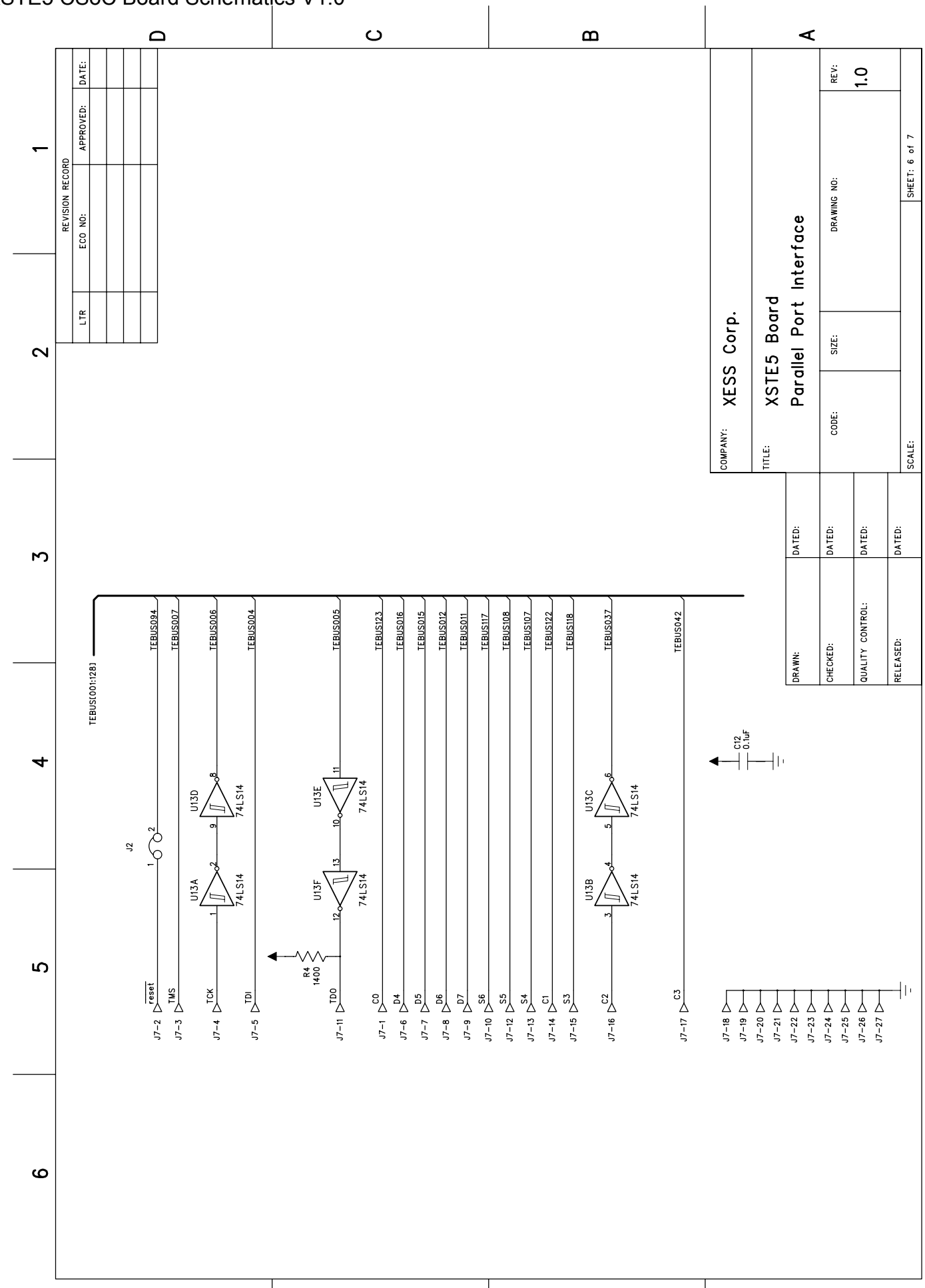

PWRPLUG
J1
CENTER
SIDE
SWITCH
D1
7805
U2
PWR
+5V
GND
IN
OUT
ADJ
U1
LM317
R1
768
R2
464
C1
10uF
10V
C2
10uF
10V
+5V
+3.3V
COMPANY: XESS Corp.
TITLE: XSTE5 Board
Power Conditioning
DRAWN:
DATED:
CHECKED:
DATED:
QUALITY CONTROL:
DATED:
RELEASED:
DATED:
CODE:
SIZE:
DRAWING NO:
REV: 1.0
SCALE:
SHEET: 1 of 7

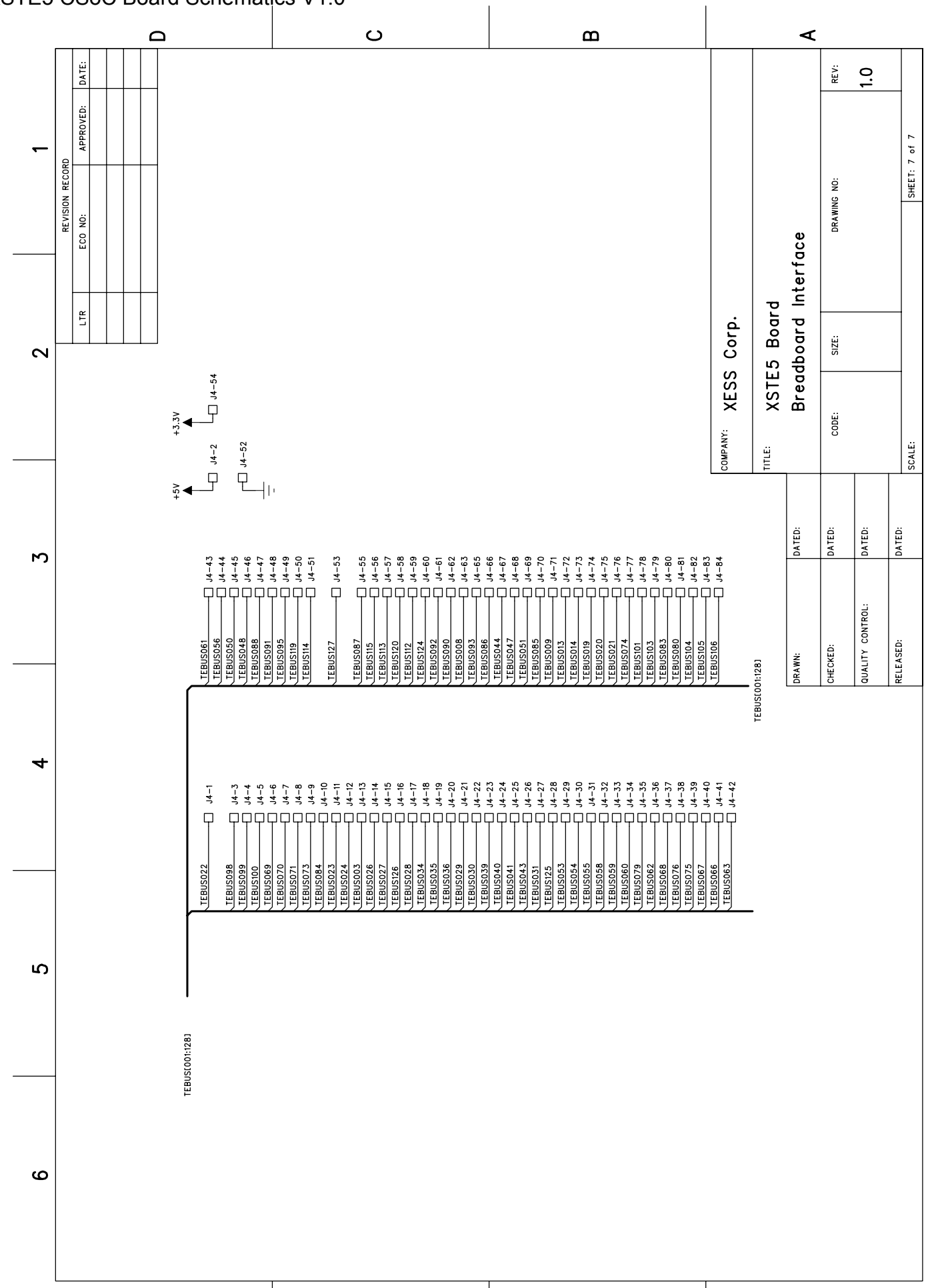

TEBUS[001:128]
TEBUS037
TEBUS003
4.7K
U14F
U14G
4.7K
I/O
OUT0
VCC
DS1075
U3
GND
OSCIN
XTAL
OE
PDN/SELX
+5V
+5V
C3
0.1uF
J4-64
COMPANY: XESS Corp.
TITLE: XSTE5 Board
Clock Generator
CODE:
SIZE:
DRAWING NO:
REV: 1.0
SCALE:
SHEET: 2 of 7
DRAWN:
DATED:
CHECKED:
DATED:
QUALITY CONTROL:
DATED:
RELEASED:
DATED:


REVISION RECORD
LTR
ECO NO:
APPROVED:
DATE:
COMPANY: XESS Corp.
TITLE: XSTE5 Board
SRAM & FLASH MEMORY
CODE:
SIZE:
DRAWING NO:
REV: 1.0
SCALE:
SHEET: 3 of 7
DRAWN:
DATED:
CHECKED:
QUALITY CONTROL:
RELEASED:
U4
128KX8_SRAM
U5
AS29F002
U14D 4.7K
U14E 4.7K
J8
J9
C4 0.1uF
C5 0.1uF
+5V
TEBUS[001:128]
TEBUS020
TEBUS093


REVISION RECORD
LTR
ECO NO:
APPROVED:
DATE:
U6
TE505
U14A 4.7K
U14B 4.7K
U14C 4.7K
C6 0.1uF
C7 0.1uF
C8 0.1uF
C9 0.1uF
C10 0.1uF
C11 0.1uF
+3.3V
COMPANY: XESS Corp.
TITLE: XSTE5 Board
Configurable System-on-Chip
DRAWN:
CHECKED:
QUALITY CONTROL:
RELEASED:
DATED:
CODE:
SIZE:
DRAWING NO:
REV: 1.0
SCALE:
SHEET: 4 of 7


REVISION RECORD
LTR
ECO NO:
APPROVED:
DATE:
COMPANY: XESS Corp.
TITLE: XSTE5 Board
VGA,LED,PS/2,Switch I/O
CODE:
SIZE:
DRAWING NO:
REV: 1.0
SCALE:
SHEET: 5 of 7
DRAWN:
CHECKED:
QUALITY CONTROL:
RELEASED:
DATED:
7-Segment LED
DIP Switch
PS/2 Port
VGA Port
TEBUS[00:1281]
data
clock
RED
green
blue
hsync
vsync


REVISION RECORD
LTR
ECO NO:
APPROVED:
DATE:
COMPANY: XESS Corp.
TITLE: XSTE5 Board
Parallel Port Interface
CODE:
SIZE:
DRAWING NO:
REV: 1.0
SCALE:
SHEET: 6 of 7
DRAWN:
CHECKED:
QUALITY CONTROL:
RELEASED:
DATED:
TEBUS[001:128]
J2
U13A
U13B
U13C
U13D
U13E
U13F
74LS14
R4
1400
C12
0.1uF
reset
TMS
TCK
TDI
TDO
C0
D4
D5
D6
D7
S6
S5
S4
C1
S3
C2
C3
TEBUS094
TEBUS007
TEBUS006
TEBUS004
TEBUS005
TEBUS123
TEBUS016
TEBUS015
TEBUS012
TEBUS011
TEBUS117
TEBUS108
TEBUS107
TEBUS122
TEBUS118
TEBUS037
TEBUS042
J7-1
J7-2
J7-3
J7-4
J7-5
J7-6
J7-7
J7-8
J7-9
J7-10
J7-11
J7-12
J7-13
J7-14
J7-15
J7-16
J7-17
J7-18
J7-19
J7-20
J7-21
J7-22
J7-23
J7-24
J7-25
J7-26
J7-27


REVISION RECORD
LTR
ECO NO:
APPROVED:
DATE:
+5V
+3.3V
J4-2
J4-52
J4-54
TEBUS001:128J
TEBUS022 J4-1
TEBUS098 J4-3
TEBUS099 J4-4
TEBUS100 J4-5
TEBUS069 J4-6
TEBUS070 J4-7
TEBUS071 J4-8
TEBUS073 J4-9
TEBUS084 J4-10
TEBUS023 J4-11
TEBUS024 J4-12
TEBUS003 J4-13
TEBUS026 J4-14
TEBUS027 J4-15
TEBUS126 J4-16
TEBUS028 J4-17
TEBUS034 J4-18
TEBUS035 J4-19
TEBUS036 J4-20
TEBUS029 J4-21
TEBUS030 J4-22
TEBUS039 J4-23
TEBUS040 J4-24
TEBUS041 J4-25
TEBUS043 J4-26
TEBUS031 J4-27
TEBUS125 J4-28
TEBUS053 J4-29
TEBUS054 J4-30
TEBUS055 J4-31
TEBUS058 J4-32
TEBUS059 J4-33
TEBUS060 J4-34
TEBUS079 J4-35
TEBUS062 J4-36
TEBUS068 J4-37
TEBUS076 J4-38
TEBUS075 J4-39
TEBUS067 J4-40
TEBUS066 J4-41
TEBUS063 J4-42
TEBUS061 J4-43
TEBUS056 J4-44
TEBUS050 J4-45
TEBUS048 J4-46
TEBUS088 J4-47
TEBUS091 J4-48
TEBUS095 J4-49
TEBUS119 J4-50
TEBUS114 J4-51
TEBUS127 J4-53
TEBUS087 J4-55
TEBUS115 J4-56
TEBUS113 J4-57
TEBUS120 J4-58
TEBUS112 J4-59
TEBUS124 J4-60
TEBUS092 J4-61
TEBUS090 J4-62
TEBUS008 J4-63
TEBUS093 J4-65
TEBUS086 J4-66
TEBUS044 J4-67
TEBUS047 J4-68
TEBUS051 J4-69
TEBUS085 J4-70
TEBUS009 J4-71
TEBUS013 J4-72
TEBUS014 J4-73
TEBUS019 J4-74
TEBUS020 J4-75
TEBUS021 J4-76
TEBUS074 J4-77
TEBUS101 J4-78
TEBUS103 J4-79
TEBUS083 J4-80
TEBUS080 J4-81
TEBUS104 J4-82
TEBUS105 J4-83
TEBUS106 J4-84
TEBUS001:128J
COMPANY: XESS Corp.
TITLE: XSTE5 Board
Breadboard Interface
DRAWN: DATED:
CHECKED: DATED:
QUALITY CONTROL: DATED:
RELEASED: DATED:
CODE:
SIZE:
DRAWING NO:
REV: 1.0
SCALE:
SHEET: 7 of 7