XESS Corporation

XStend Board V3.0 Manual

How to install and use
your new XStend Board

RELEASE DATE: 09/30/2008

Table of Contents

1 Preliminaries

Getting Help!

If you can't get the XStend Board hardware to work, submit a problem report at http://www.xess.com/help.html. Our web site also has:

- the XStend 3.0 Board product page,
- answers to frequently-asked-questions,
- example designs for the XS Boards,
- application notes,
- a place to sign-up for our email forum where you can post questions to other XS Board users.

Take notice!!

- The XStend Board V3.0 is **not compatible** with the XS95, XS40 or XSTE5 Boards! Do not plug XS95, XS40 or XSTE5 Boards into the XStend Board V3.0!
- If you are connecting a power adapter to jack J7 of your XStend Board, please make sure the center terminal of the plug is positive and the outer sleeve is negative!

Packing List

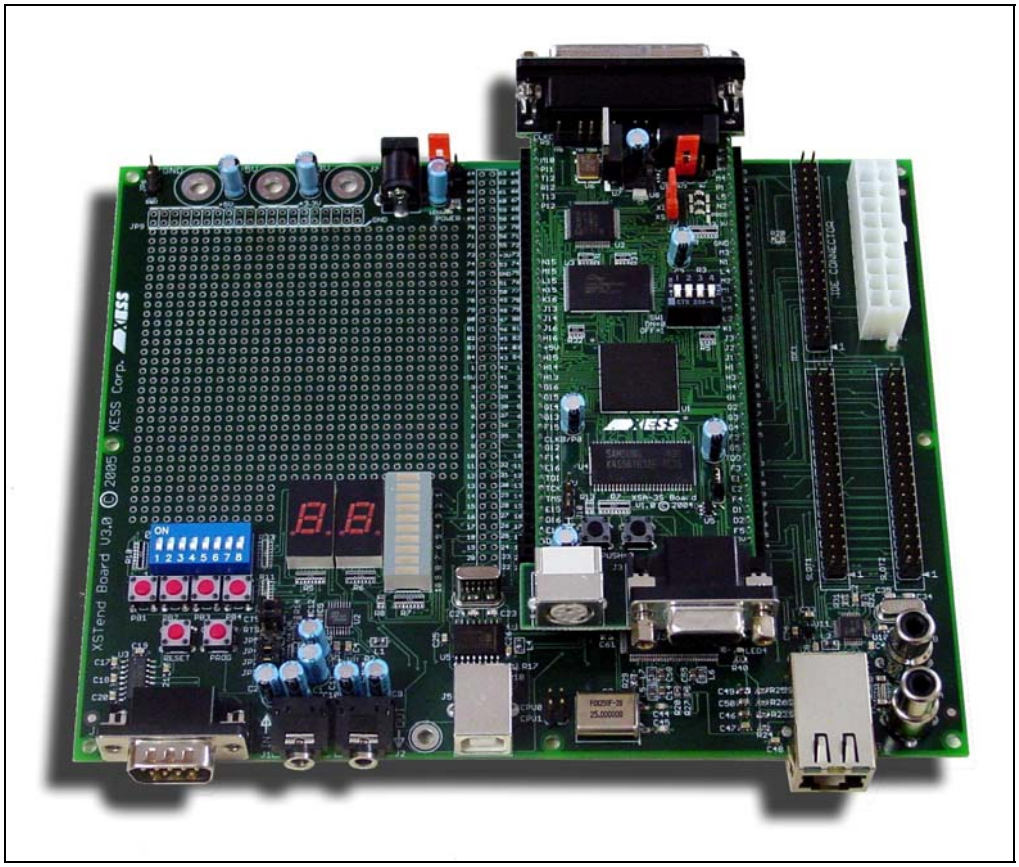
Here is what you should have received in your package:

- an XStend Board;
- an XSTOOLs CDROM with software utilities and documentation for using the XStend Board.

2 Installation

Inserting the XSA Board into an XStend Board

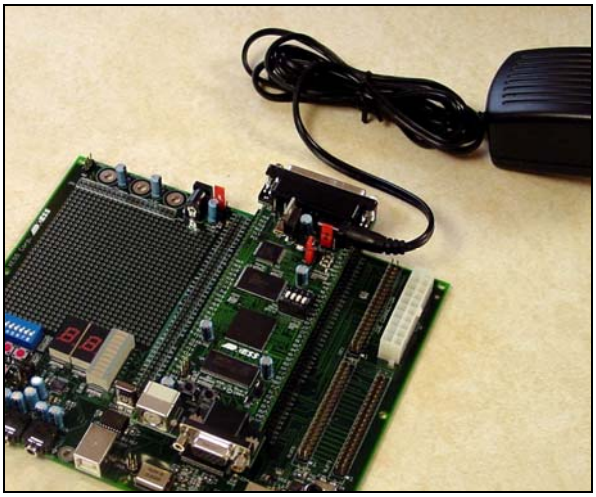
The XSA Board is inserted into the XStend Board as shown below. The XSA Board is inserted into the innermost columns of the socket strips. **Orient the parallel port, VGA port and PS/2 port connectors on the XSA Board as indicated on the XStend Board!!**



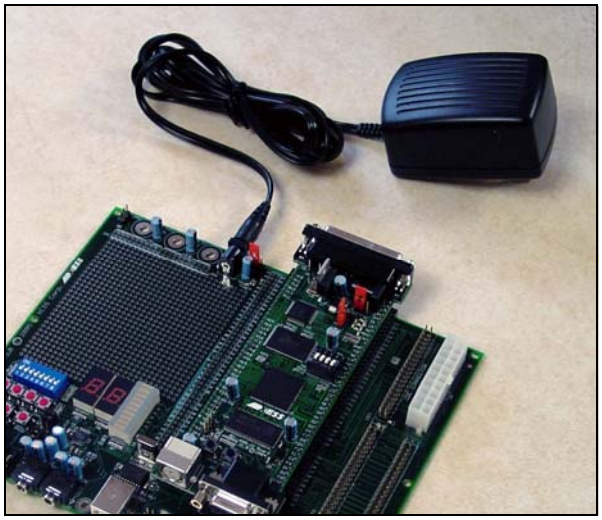
Applying Power to Your XStend Board

You can supply power to your XStend Board in four ways. **Do not apply power from more than one source at a time!!**

You can power both the XStend Board and your XSA Board by attaching a DC power supply to your XSA Board as shown below. The XStend Board will draw its power through the XSA Board prototyping header. (The 5V output from the XSA Board can only supply a few mA to the XStend Board, so you should use one of the other methods to power the board if you are attaching 5V logic to the XStend Board.)

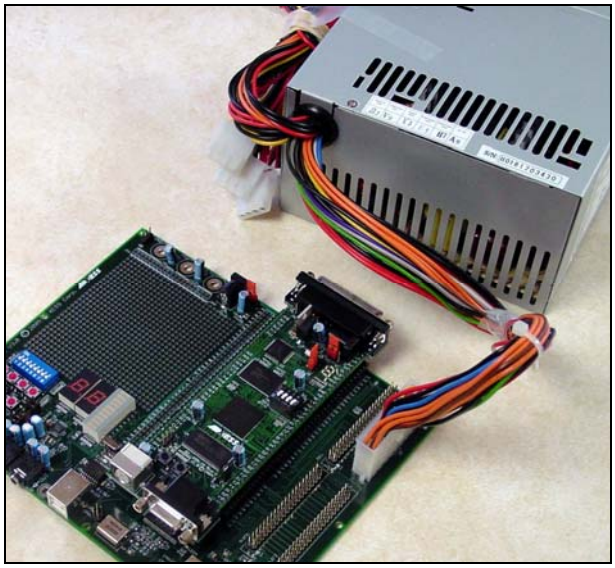


Or you can attach a 5V or 9V DC power supply directly to jack J7 on the XStend Board. Now the XSA Board will draw its power from the XStend Board. (Place the shunt on jumper JP1 in the appropriate position for the voltage of your power supply. **Applying 9V will damage your XStend and XSA Boards if the shunt is in the 5V position!**)

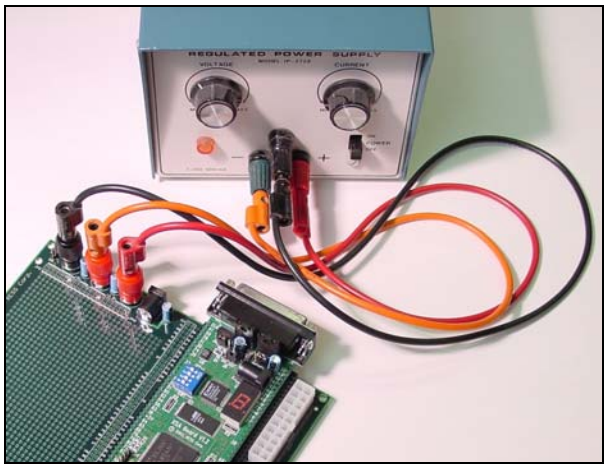


Or you can attach a standard ATX PC power supply to the XStend Board through connector J6. Place the shunt on jumper JP1 in the +5V position. If using the XStend

Board with an XSA-3S1000, place the shunt on jumper J7 of the XSA-3S1000 Board in the PS/2 position.



Finally, you can power the XStend Board from a dual 5V / 3.3V power supply directly to binding posts on the XStend Board. (The binding posts are not provided.) Place the shunt on jumper JP1 in the +5V position. If using the XStend Board with an XSA-3S1000, place the shunt on jumper J7 of the XSA-3S1000 Board in the PS/2 position.



Making Connections to Your XSA and XStend Boards

You can make the same connections to your XSA Board whether it is inserted into the XStend Board or used stand-alone. The download cable attaches from the parallel port on the PC to the female DB-25 connector (J8) at the top of the XSA Board. You can connect a VGA monitor to the 15-pin connector (J3) at the bottom of your XSA Board. And a keyboard or mouse connects through the PS/2 connector (J4).

The XStend Board offers some additional connection opportunities:

- You can capture audio output from a CD player or a microphone by attaching them to the 3.5mm stereo input jack (J1) on the XStend Board, while audio can be sent to a pair of headphones through the stereo output jack (J2).
- You can also grab frames of NTSC, PAL or SECAM video by piping them into one of the RCA connectors (AIP1A and AIP1B).
- You can perform serial communications by attaching a cable between the DB9 connector (J9) on the XStend Board and a PC serial port.
- You can send and receive USB packets by connecting the peripheral end of a USB 1.1 cable to the USB port (J5) on the XStend Board while the host end attaches to a PC USB port.
- You can send and receive Ethernet packets by inserting a Category 5 cable with a male RJ45 connector into the RJ45 female connector (X3).
- You can place data in long-term storage by connecting a hard drive to the 40-pin IDE connector (IDE1).
- You can add functions by attaching external modules to the 40-pin daughterboard connectors (SLOT1 and SLOT2).

Setting the Jumpers on Your XStend Board

The default jumper settings shown in Table 1 configure your XStend Board for use in a logic design environment. You will need to change the jumper settings only if you are:

- powering the board from a regulated 5V supply applied through jack J7,
- accepting audio signals from a low-amplitude source (e.g., a passive microphone),
- attaching a null modem cable from a PC to the serial port connector J9,
- disconnecting the RTS and CTS serial port signals,
- changing the bus interface to the Ethernet MAC+PHY chip.

- Table 1: Jumper settings for XStend Board.

Jumper	Setting	Purpose
JP1	+9V (default)	Place the shunt in this position if you are applying a voltage greater than 7V through power jack J7.
	+5V	Place the shunt in this position if you are applying a voltage of exactly 5V from a regulated power supply through power jack J7.
JP2	Off (default)	Removing this shunt interrupts power to a passive microphone attached to the left stereo input channel.
	On	Placing a shunt on this jumper provides power to a passive microphone attached to the left stereo input channel.

Jumper	Setting	Purpose
JP3	Off (default)	Removing this shunt interrupts power to a passive microphone attached to the right stereo input channel.
	On	Placing a shunt on this jumper provides power to a passive microphone attached to the right stereo input channel.
JP4	Off	Removing this shunt sets the gain on the left stereo input channel to 48.
	On (default)	Placing a shunt on this jumper sets the gain on the left stereo input channel to 1.
JP5	Off	Removing this shunt sets the gain on the right stereo input channel to 48.
	On (default)	Placing a shunt on this jumper sets the gain on the right stereo input channel to 1.
JP7	1–2, 3–4, 5–6, 7–8	Placing the shunts on these pins makes the XStend Board appear as a DTE device so it must be connected to the PC serial port using a null modem cable.
	1–3, 2–4, 5–7, 6–8	Placing the shunts on these pins makes the XStend Board appear as a DCE device so it must be connected to the PC serial port using a straight-through cable.
RTS	Off	Removing this shunt disconnects the XSA Board from the RTS signal of the serial interface.
	On (default)	Placing a shunt on this jumper connects the XSA Board to the RTS signal of the serial interface.
CTS	Off	Removing this shunt disconnects the XSA Board from the CTS signal of the serial interface.
	On (default)	Placing a shunt on this jumper connects the XSA Board to the CTS signal of the serial interface.
CPU1, CPU0	Off, Off	Places the Ethernet chip bus interface into 8051 mode.
	Off, On	Places the Ethernet chip bus interface into 68K mode.
	On, Off	Places the Ethernet chip bus interface into x86 mode.
	On, On	Places the Ethernet chip bus interface into ISA mode.

3

XStend Board Interfaces

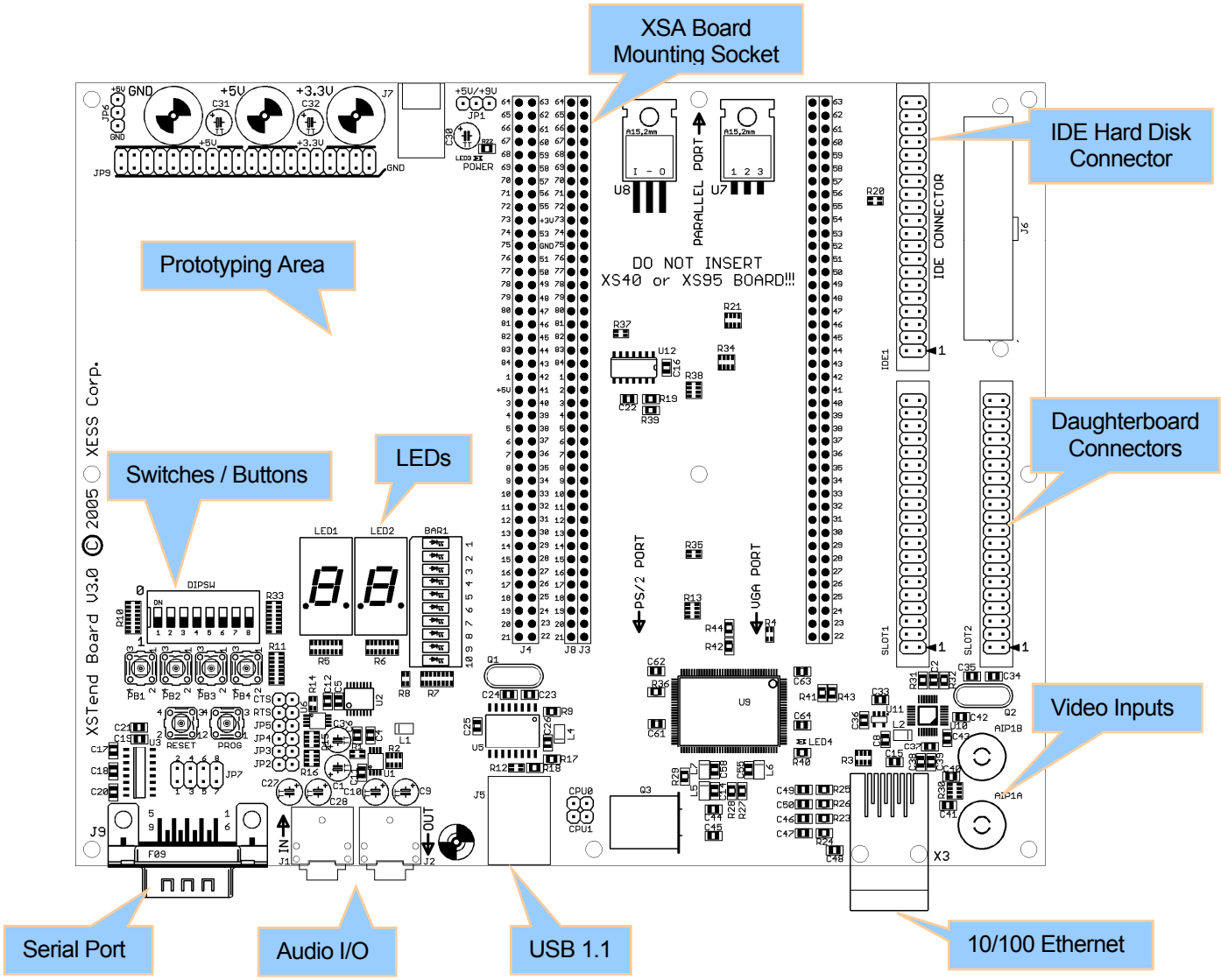
This section describes the various sections of the XStend Board and shows how the FPGA on the XSA Board interfaces to the various components of the XStend Board. Please refer to the complete schematics and pin list at the end of this document if you need more details.

XStend Board Capabilities

The XSA Boards offer a flexible, low-cost method of prototyping FPGA designs. However, their small physical size limits the amount of support circuitry they can hold. The XStend Board extends the range of applications of the XSA Boards by providing additional support circuitry such as:

- mounting sockets that provide the main interface between the FPGA on the XSA Board and the XStend Board components;
- additional bargraph LED and LED digits for use as simple output devices;
- DIP switches and pushbuttons that serve as simple input devices;
- a stereo codec with left/right input/output channels for audio DSP applications;
- a video decoder that digitizes NTSC/PAL/SECAM signals for input to image processing applications;
- an RS-232 serial port for sending information over a low-speed communication link;
- a USB 1.1 interface that lets the FPGA appear as a low-speed or full-speed USB peripheral device;
- a 10/100 Base-T Ethernet interface that supports various network communication protocols such as TCP/IP;
- an IDE hard disk interface that gives the FPGA access to long-term, nonvolatile data storage;
- dual 20×2 daughterboard headers allow the addition of external modules with new capabilities;
- a 2.75"×2.75" prototyping area where custom circuitry can be built.

The locations of the circuitry that provide these new capabilities are indicated on the following layout. Each of these components and their interconnections will be described in the following sections.



XStend Board Components

Interconnection Buses

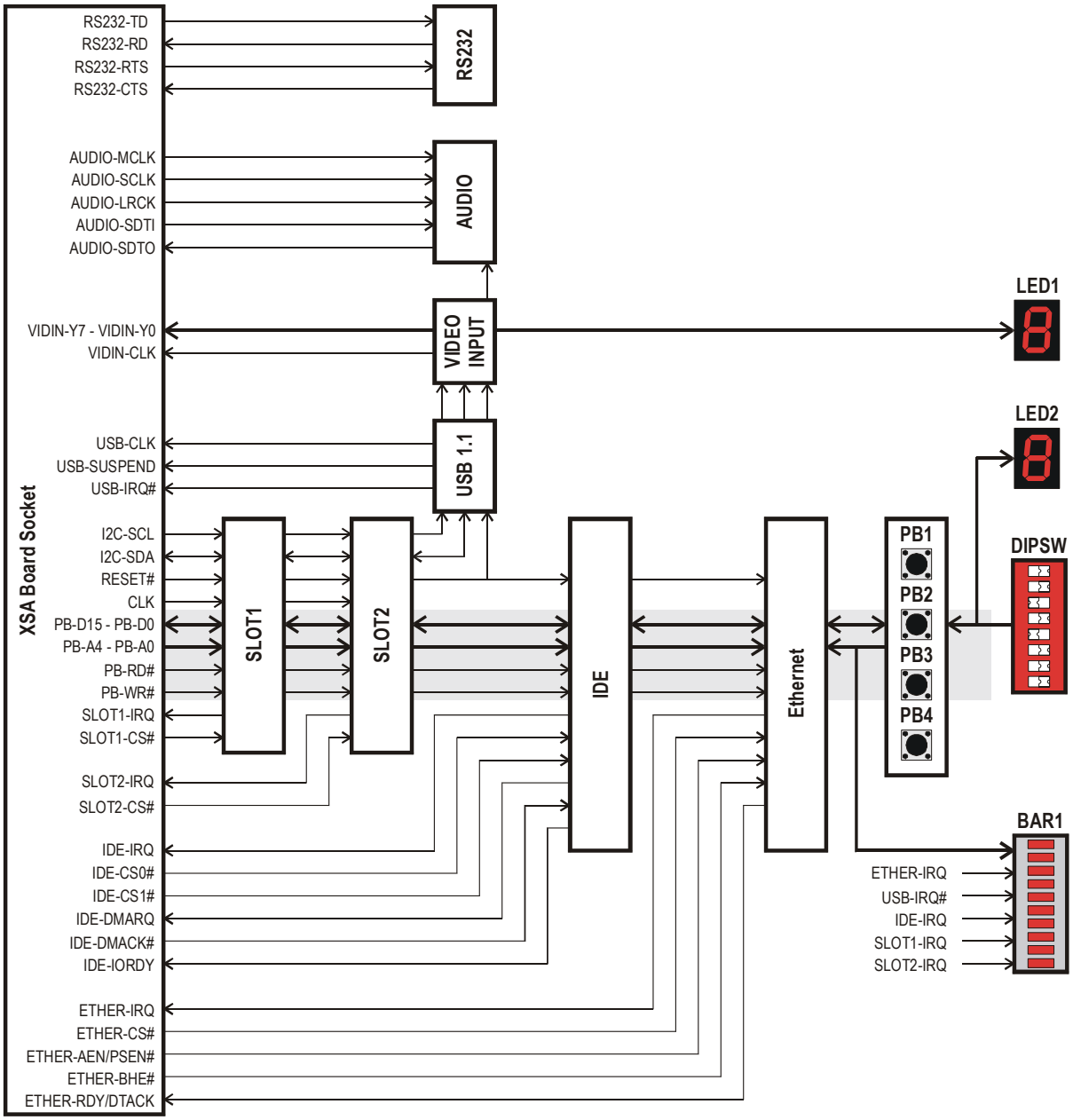
The connections between the various components on the XStend Board are shown below. The socket for the XSA Board connects to the other components through a peripheral bus, I2C bus, and several point-to-point dedicated buses.

The peripheral bus consists of sixteen data lines, five address lines, and two read/write strobes that form the main data conduit between the FPGA and the Ethernet interface, IDE interface, both daughterboard headers and most of the switches, pushbuttons and

LEDs. The chip-selects for components on the peripheral bus are controlled by the FPGA to prevent contention. These devices also have sideband signals for interrupts and other status/control functions that are specific to their operations.

The I^2C bus consisting of a clock line and a data line connects the FPGA to the USB interface, video decoder and both daughterboard headers. For the video decoder it serves only to send register setup data, but it is the main conduit for packets going through the USB interface. Its function for any daughterboards is dependent on the characteristics of the external modules.

The components that process video/audio streams and handle the serial port use dedicated point-to-point buses.



XSA Board Mounting Sockets

The FPGA on the XSA Board accesses the functions of the XStend Board by mating its prototyping header with the XStend Board mounting socket. The XSA Board is mounted using the inner rows of the double-row sockets.

In addition, the outer rows of each socket provide access points for probing the signals that go through the sockets. Each hole in the outer rows is electrically connected to the horizontally adjacent hole on the inner rows. Small wires (22-gauge or less) can be inserted in the holes on the outer rows and logic or oscilloscope probes can be attached to monitor the signals going through the mounting socket.

LEDs

The XStend Board has a ten-segment bargraph LED and two seven-segment LED displays. All of these LEDs are active-high meaning that an LED segment will glow when a high logic level is applied to it.

These LEDs are connected on the XStend Board as follows:

LED Segment	XStend Connection	LED Segment	XStend Connection
BAR1	PB-A0	LED1-D	VIDIN-Y3
BAR2	PB-A1	LED1-E	VIDIN-Y4
BAR3	PB-A2	LED1-F	VIDIN-Y5
BAR4	PB-A3	LED1-G	VIDIN-Y6
BAR5	PB-A4	LED1-DP	VIDIN-Y7
BAR6	ETHER-IRQ	LED2-A	PB-D8
BAR7	USB-IRQ#	LED2-B	PB-D9
BAR8	IDE-IRQ	LED2-C	PB-D10
BAR9	SLOT1-IRQ	LED2-D	PB-D11
BAR10	SLOT2-IRQ	LED2-E	PB-D12
LED1-A	VIDIN-Y0	LED2-F	PB-D13
LED1-B	VIDIN-Y1	LED2-G	PB-D14
LED1-C	VIDIN-Y2	LED2-DP	PB-D15

The bargraph LED segments share their connections with the lines of the peripheral address bus and the interrupt outputs from other devices on the XStend Board. The LEDs are not latched so they will respond to any signal driven on these lines. The interrupt outputs from the other devices are protected by current-limiting resistors so they will not be damaged if the FPGA actively drives the bargraph LEDs. (No current-limiting resistors are needed on the address bus because the FPGA is the only device that can drive these lines.)

The segments of the LED1 seven-segment display share their connections with the pixel output bus of the video decoder. The LEDs are not latched so they will respond to any signal driven on these lines. There are no current-limiting resistors on the pixel bus, so the video decoder must be configured to place its outputs in a high-impedance state whenever the FPGA drives the LED1 segments. (Upon power-up or after a system reset,

the video decoder outputs are in a high-impedance state by default. The video decoder must receive an explicit command over the I^2C bus before it will activate these outputs.)

The segments of the LED2 seven-segment display share their connections with the upper byte of the peripheral data bus. The LEDs are not latched so they will respond to any signal driven on these lines. There are no current-limiting resistors on the peripheral data bus, so the chip-selects for the other devices on the peripheral data bus must be deactivated whenever the FPGA drives the LED1 segments.

DIP Switch and Pushbuttons

The XStend has a bank of eight DIP switches and four pushbuttons that are accessible by the XSA Board. When a DIP switch is closed or a pushbutton is pressed, the corresponding signal line is pulled to ground. When a DIP switch is open or a pushbutton is released, the signal line is pulled to a high level through a resistor.

The pushbuttons and switches are connected on the XStend Board as follows:

Pushbuttons / Switches	XStend Connection	Pushbuttons / Switches	XStend Connection
PB1	PB-D15	DIPSW-3	PB-D2
PB2	PB-A0	DIPSW-4	PB-D3
PB3	PB-A1	DIPSW-5	PB-D4
PB4	PB-A2	DIPSW-6	PB-D5
DIPSW-1	PB-D0	DIPSW-7	PB-D6
DIPSW-2	PB-D1	DIPSW-8	PB-D7

When the FPGA reads the state of the switches or pushbutton PB1, it must deactivate the chip-selects of the other devices on the peripheral data bus so they will not interfere. This is not necessary when reading the state of pushbuttons PB2, PB3 and PB4 because they are attached to the address bus and only the FPGA can drive these lines. (Instead of simple output-only drivers, you will have to use bidirectional I/O drivers for the peripheral address bus if you want the FPGA to read the state of these pushbuttons.)

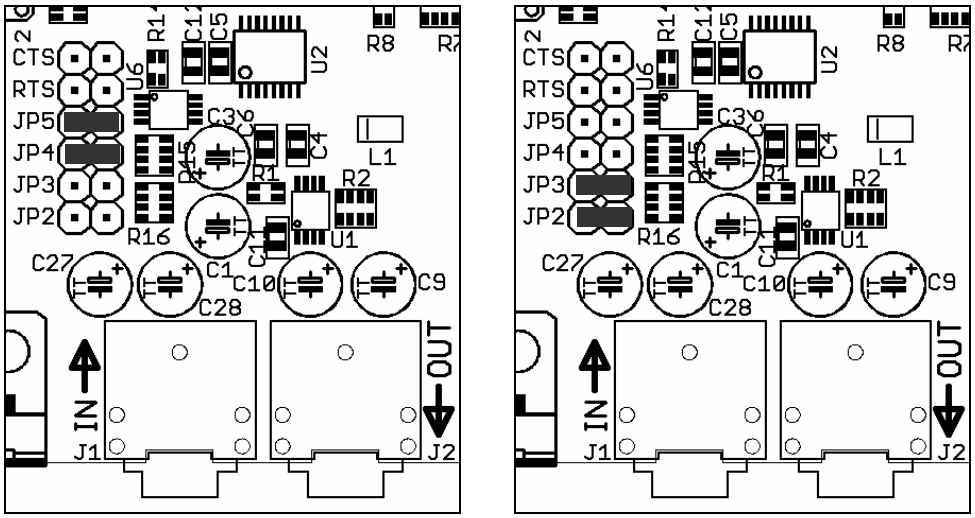
Current-limiting resistors are placed between the switches/pushbuttons and the peripheral bus lines to prevent damage if another device drives these lines at the same time that a switch or pushbutton is closed. In such cases, the level driven by the other device overrides the level from the pushbutton or switch.

Stereo Audio Codec

The XStend Board has a stereo audio codec (AKM AK4551) that accepts two analog input channels, digitizes the analog values, and sends the digital values to the FPGA as a serial bit stream on the AUDIO-SDTO signal line. The codec also accepts a serial bit stream from the FPGA on the AUDIO-SDTI signal line and converts it into two analog output signals that exit the XStend Board. The AUDIO-MCLK, AUDIO-SCLK and AUDIO-LRCK serve as clock signals that control the sequencing of the serial data streams.

The analog stereo input and output signals enter and exit the XStend Board through the 3.5mm jacks J1 and J2, respectively. A soundcard, CD player or passive microphone

provides a source of audio through J1, and a set of small stereo headphones can be connected to J2 for listening to the processed output. The shunts on jumpers JP2–JP5 should be positioned as shown in the left-hand figure if you are using a high-powered audio signal that doesn't require amplification (e.g., a soundcard or CD player), while the shunt positions shown in the right-hand figure allow the audio circuit to amplify and provide power to a passive microphone.



Video Decoder

The XSB Board can digitize NTSC, SECAM, and PAL video signals using a video decoder chip (Texas Instruments TVP5150A). Eight-bit pixels of digitized video arrive at the FPGA over the VIDIN-Y bus on the rising edge of the VIDIN-CLK (which is generated by the video decoder chip). The FPGA programs the video decoder options by reading and writing registers through the I^2C bus at I^2C address 0x5C.

The connections of the video decoder signals to the XStend Board are as follows:

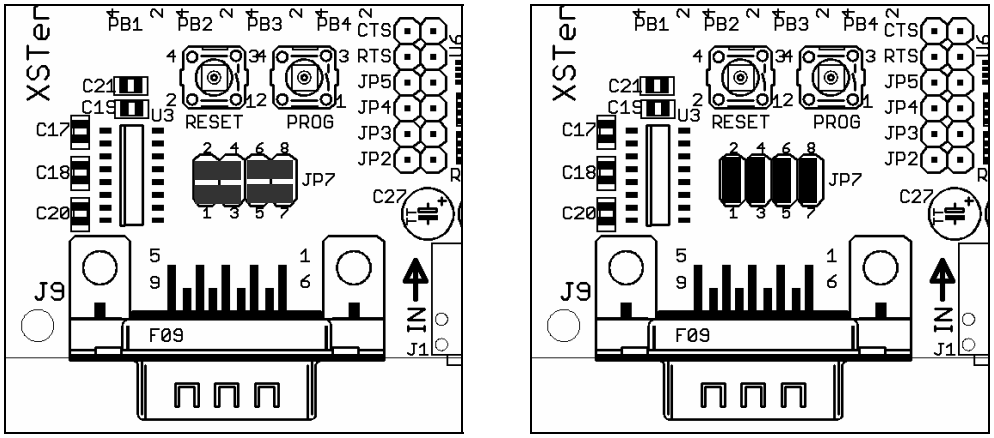
Video Decoder	XStend Board	Video Decoder	XStend Board
PCLK/SCLK	VIDIN-CLK	YOUT6	VIDIN-Y6
YOUT0	VIDIN-Y0	YOUT7	VIDIN-Y7
YOUT1	VIDIN-Y1	INTERQ/GPCL	VIDIN-IRQ
YOUT2	VIDIN-Y2	HSYNC	VIDIN-HSYNC
YOUT3	VIDIN-Y3	VSYNC/PALI	VIDIN-VSYNC
YOUT4	VIDIN-Y4	FID/GLCO	VIDIN-FID
YOUT5	VIDIN-Y5	AVID	VIDIN-AVID

The VIDIN-IRQ, VIDIN-HSYNC, VIDIN-VSYNC, VIDIN-FID and VIDIN-AVID signals are not made available to the FPGA on some XSA Board models. For these boards, the equivalent functions are performed using the embedded sync flags inserted into the pixel stream according to the ITU-R BT.656 standard.

RS-232 Serial Port

The XStend Board has a 9-pin RS-232 port that provides the FPGA with transmit and receive serial data streams (TD and RD) as well as flow control signals (RTS and CTS).

The shunts on jumper JP7 should be set as shown in the left-hand picture if you are connecting the XStend Board to a PC through a straight-through serial cable. The shunts should be placed as shown in the right-hand figure if you are using a null-modem cable.



When using the XStend Board with an XSA-50 or XSA-100 Board, the RTS and CTS signals share the same wiring that is used by the PS/2 connector. Therefore, if you are using a mouse or keyboard with an XSA-50 or XSA-100 Board, you must remove the shunts on the RTS and CTS jumpers to keep these signals from interfering with the PS/2 port. The RTS and CTS signals do not share the PS/2 port wiring on other models of the XSA Board, so the shunts can remain in place.

USB 1.1 Interface

The XStend Board uses a USB-to-I^2C interface chip (Philips PDIUSBD11) to provide the XSA Board with a USB communication link. The FPGA accesses registers on the chip via the I^2C bus at the seven-bit I^2C addresses 0x1A and 0x1B. By reading and writing these registers, the FPGA can act as a USB peripheral with the USB interface chip handling the low-level data transactions for the USB bus. The USB interface chip also provides an interrupt signal to alert the FPGA when USB transactions need to be processed.

In addition, a suspend signal is output from the chip to alert the FPGA when the USB bus loses power or otherwise ceases operations. A clock output from the chip is also made available to the FPGA. The frequency of this clock is 48 MHz / (N+1) where N is a value loaded into a register on the chip through the I^2C interface. (The suspend and clock signals are not available if you use an XSA-50 or XSA-100 Board with the XStend Board.)

10/100 Ethernet Interface

The XSB Board sends data over an Ethernet LAN at 10 or 100 Mbps through an Ethernet MAC+PHY chip (ASIX AX88796). The FPGA controls the Ethernet chip by reading and writing registers and FIFO buffers on the chip through a standard microprocessor bus interface.

The Ethernet chip supports several microprocessor bus interfaces. The interface is chosen by setting the shunts on jumpers CPU0 and CPU1 as follows:

Microprocessor Interface	Shunt Settings	
	CPU1	CPU0
MCS-51 (805X)	OFF	OFF
MC68K	OFF	ON
80186	ON	OFF
ISA Bus	ON	ON

The connections of the Ethernet chip to the XStend Board are as follows:

MAC+PHY	XStend Connection	MAC+PHY	XStend Connection
CS#	ETHER-CS#	SD4	PB-D4
IOR#	PB-OE#	SD5	PB-D5
IOW#	PB-WE#	SD6	PB-D6
AEN/PSEN	ETHER-AEN/PSEN#	SD7	PB-D7
BHE#	ETHER-BHE#	SD8	PB-D8
SA0	PB-A0	SD9	PB-D9
SA1	PB-A1	SD10	PB-D10
SA2	PB-A2	SD11	PB-D11
SA3	PB-A3	SD12	PB-D12
SA4	PB-A4	SD13	PB-D13
SD0	PB-D0	SD14	PB-D14
SD1	PB-D1	SD15	PB-D15
SD2	PB-D2	IREQ	ETHER-IRQ
SD3	PB-D3	RDY/DTACK	ETHER-RDY/DTACK

IDE Interface

The FPGA can access a hard disk through the 40-pin IDE interface connector. The FPGA stores and retrieves data from the disk by reading and writing registers on the disk through the IDE interface. These registers are accessed using the read and write strobes in combination with the register bank chip-select lines, the three-bit register address bus and the sixteen-bit data bus.

In addition to polled access, the IDE interface also allows DMA access using the DMA request and acknowledge signals along with the I/O ready signal.

The connections of the IDE interface signals to the XStend Board are as follows:

IDE Interface	XStend Connection	IDE Interface	XStend Connection
CS0#	IDE-CS0#	DD7	PB-D7
CS1#	IDE-CS1#	DD8	PB-D8
DA0	PB-A0	DD9	PB-D9
DA1	PB-A1	DD10	PB-D10
DA2	PB-A2	DD11	PB-D11
DIOR#	PB-RD#	DD12	PB-D12
DIOW#	PB-WR#	DD13	PB-D13
DD0	PB-D0	DD14	PB-D14
DD1	PB-D1	DD15	PB-D15
DD2	PB-D2	INTRQ	IDE-IRQ
DD3	PB-D3	DMARQ	IDE-DMARQ
DD4	PB-D4	DMACK#	IDE-DMACK#
DD5	PB-D5	IORDY	IDE-IORDY
DD6	PB-D6		

Daughterboard Headers

Daughterboards with specialized circuitry can be connected to the XStend board through the 20×2 headers SLOT1 and SLOT2.

The official functions of the signals attached to the daughterboard headers are as follows:

MASTER-RESET#: An active-low signal that is used to reset the daughterboard to a known state.

CLK: A clock signal sent by the FPGA for synchronizing the daughterboard operations.

PB-D15 – PB-D0: The 16-bit bidirectional peripheral data bus.

PB-A4 – PB-A0: The 5-bit peripheral address bus is used to address up to 32 locations on a daughterboard.

PB-RD#: An active-low read strobe that enables the daughterboard to send data over the peripheral bus. This signal can be used in conjunction with the CLK signal to perform synchronous reads.

PB-WR#: An active-low write strobe that enables the daughterboard to receive data from the peripheral bus. This signal can be used in conjunction with the CLK signal to perform synchronous writes.

SLOT1-CS#, SLOT2-CS#: An active-low chip-select that enables the daughterboard to access the peripheral bus for read and write operations. Each daughterboard has a dedicated chip-select.

SLOT1-IRQ, SLOT2-IRQ: An active-high interrupt generated by the daughterboard to signal the FPGA that some action needs to be taken. Each daughterboard has a dedicated interrupt line.

I2C-SCL, I2C-SDA: The clock and data lines for the I^2C bus that can be used to access any devices on the daughterboard with I^2C interfaces.

Except for the MASTER-RESET# signal, all of the daughterboard signals connect directly to the FPGA. Therefore, you can use them to perform any function you want as long as you follow some simple rules:

- The daughterboard should never actively drive its CLK or SLOT-CS# signal.
- The daughterboard should never actively-drive any of its signals (except for the SLOT-IRQ signal) when its SLOT-CS# signal is high.

Prototyping Area

The XStend Board has a prototyping area consisting of component through-holes on an 0.1"×0.1" grid. Components in this area can access to the +5V, +3.3V and signal ground by making connections to the appropriate pins on the JP9 header.

Connections from the XSA Board to the prototyping area are made through the J4 header. Each pin on J4 is explicitly labeled with the corresponding number of the prototyping header pin it connects to on the XSA Board. For example, the pin at the bottom-left of J4 on the XStend Board is connected to pin 21 of the XSA Board prototyping header.

Reset Circuitry

Pressing the RESET button on the XStend Board will send a reset signal to the Ethernet interface, IDE interface, USB interface, video decoder, audio codec, daughterboards and the FPGA on the XSA Board. The FPGA can also initiate a reset by driving the RESET-TRIGGER# signal to a low level. A current-limiting resistor is placed between the RESET button and the FPGA to prevent damage if they simultaneously try to drive the reset to opposite levels.

Pressing the PROG button will place a low level on the PROGRAM# pin of the FPGA and erase its configuration. Only the FPGA on the XSA Board will be affected; the devices on the XStend board will retain their current settings.

Interactions Between the XSA-50,-100 Boards and the XStend Board

Many of the FPGA pins on the XSA-50 and XSA-100 Boards are connected to two or more components on the XSA and/or XStend Board. This causes interactions that may make it difficult or impossible to employ these components in the same application. This section will provide an overview of some of the possible interactions between the components. These discussions are overly pessimistic in terms of what components cannot be used together in a single application, so advanced users are encouraged to check the list of pin assignments in Appendix A for more details.

(Other models of the XSA Board have dedicated I/O pins that connect the FPGA to the prototyping header so they do not have the interactions and restrictions listed below.)

XSA-50,-100 Pushbutton Interactions

The pushbutton on the XSA-50,-100 Board shares an FPGA pin with the data line of the PS/2 port and the CTS line of the RS-232 port on the XStend Board. Therefore, these components cannot be used simultaneously.

XSA-50,-100 PS/2 Port Interactions

The clock and data line of the PS/2 port on the XSA-50,-100 Board share FPGA pins with the RTS and CTS lines of the RS-232 port on the XStend Board. The pushbutton on the XSA-50,-100 Board also shares the PS/2 data line. Therefore, these components cannot be used simultaneously.

XSA-50,-100 VGA Port Interactions

The VGA port of the XSA-50,-100 Board uses the same FPGA pins that connect to the upper-byte of the peripheral data bus, the LED2 seven-segment display, and the pushbutton PB1 on the XStend Board. Therefore, these components cannot be used simultaneously.

XSA-50,-100 DIP Switch Interactions

The DIP switch on the XSA-50,-100 Board shares FPGA pins with the interrupt lines from the USB interface, IDE interface and the two daughterboards. These interrupt lines also connect to segments of the bargraph LED. Therefore, the XSA-50,-100 Board DIP switches should be left in the OFF (OPEN) position if interrupts from these components or the bargraph LEDs are being used.

XSA-50,-100 Flash RAM Interactions

The Flash RAM on the XSA-50,-100 Board shares FPGA pins with the LED1 seven-segment display, bargraph LED, video decoder, stereo audio codec, DIP switch, pushbuttons (PB2, PB3 and PB4), the lower byte of the peripheral data bus, the peripheral address bus, and the interrupt lines for the Ethernet interface, USB interface, IDE interface and daughterboards on the XStend Board.

The Flash RAM can be deselected via its individual chip-select signal, so it can be used with the other components that share the peripheral bus, such as the IDE interface, Ethernet interface and daughterboards. (However, the interrupt lines from these components cannot be used.)

The video decoder, audio codec and interrupt lines need continuous monitoring, so they cannot be used in an application that employs the Flash RAM.

The DIP switches, pushbuttons and LEDs can be used whenever the Flash RAM is not being accessed.

These restrictions do not apply if the Flash RAM is only used to load a configuration into the FPGA on the XSA-50,-100 Board during system start-up. The other components

should not be active until after the FPGA is configured, after which the Flash RAM will be disabled so interference is not possible.

XSA-50,-100 Parallel Port Interface Interactions

The standard parallel port interface programmed into the CPLD on the XSA-50,-100 Board (dwnldpar.svf) will actively drive pins of the FPGA that also connect to the video decoder, the read and write strobes of the peripheral bus, and the interrupt line of the Ethernet interface.

The alternate parallel port interface (dwnldpa2.svf) can be downloaded into the CPLD so it will not interfere with these components but still allows bitstreams to be downloaded to the FPGA using GXSLOAD or XSLOAD. (Uploading and downloading the SDRAM, however, is not possible in this case.)

The Parallel Cable III interface for the CPLD (p3jtag.svf) allows you to use the XILINX iMPACT programming utility to configure the FPGA on the XSA Boards. This interface uses some of the same FPGA pins used by the audio codec interface on the XStend Board. Therefore, the audio codec can't be used if iMPACT is used to configure the FPGA.

XSA-50,-100 Seven-Segment LEDs Interactions

The seven-segment LED on the XSA Board shares FPGA pins with the XStend Board DIP switch and the lower byte of the peripheral data bus. Therefore, the LED can only be used when components on the peripheral data bus are not being accessed and the DIP switch is not being read. (The DIP switches do not have to be left in the OPEN position in order to use the LED because there are current limiting resistors that prevent any possible contention.)

XSA-50,-100 SDRAM Interactions

The synchronous DRAM chip on the XSA-50,-100 Board does not share any FPGA pins with any other components. Therefore, any application can use the SDRAM regardless of the other components that are to be used.

that are already being driven on the SRAM.

A

XStend + XSA Pin Connections

The following table lists the connections between the XStend Board components and the various XSA Board models. The columns of the table are arranged as follows:

Column1 is the index of the prototyping header pin on the XSA Board and the mating socket on the XStend Board. Pin 1 is in the middle of the left-hand row of pins and the pin number increases as you proceed counter-clockwise around the header or socket. (The header pin number should not be used when you create pin assignment constraints for your FPGA design.)

Column 2 is the name of the signal net in the XStend Board schematics. The prefix of each net name indicates the component to which it is connected (except for the peripheral bus, PB, that connects to many of the components).

Column 3 lists the direction of flow on a signal net as seen from the perspective of the XSA Board. Outputs are driven by the XSA Board into the XStend Board; inputs are driven by the XStend Board into the XSA Board.

Columns 4 and 5 indicate the nets that connect to the LEDs, DIP switches and pushbuttons on the XStend Board.

Columns 6–9 list the connections of the various components on the XSA-50 and XSA-100 Boards to the signal nets of the XStend Board. Column 6 lists the pin numbers that should be used to create pin assignment constraints for the FPGA on the XSA-50 or XSA-100 Board.

Column 10 lists the pin names of the FPGA on the XSA-200 Board along with the XStend Board net they connect to. The other components on the XSA-200 Board are not listed because they have no connection to the prototyping header.

Column 11 lists the pin names of the FPGA on the XSA-3S1000 Board along with the XStend Board net they connect to. The other components on the XSA-3S1000 Board are not listed because they have no connection to the prototyping header.

Connections Between the XST-3.0 Board and the Various XSA Boards

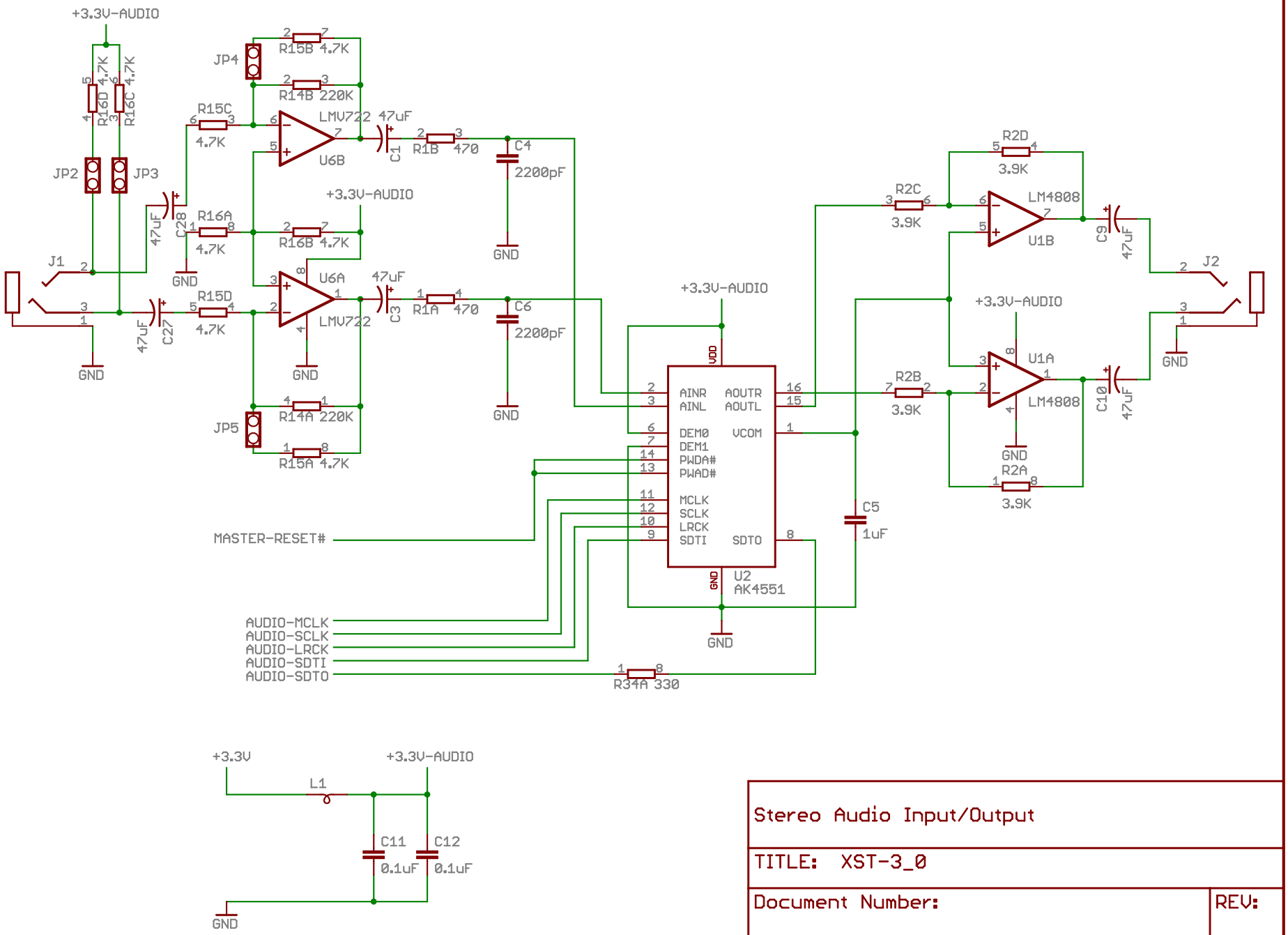
XStend Board					XSA-50 and XSA-100				XSA-200	XSA-3S1000
Proto. Pin	Net Name	Direction	LEDs	Switches	FPGA Pin	CPLD Pin	Misc. Functions		FPGA Pin	FPGA Pin
52	GND				GND				GND	GND
22	+2.5V				+2.5V				+2.5V	+2.5V
54	+3.3V				+3.3V				+3.3V	+3.3V
2	+5V				+5V				+5V	+5V
69	AUDIO-LRCK	OUT			30 (WR#)	19			G14	R12
67	AUDIO-MCLK	OUT			78		PP-S6		H13	P11
68	AUDIO-SCLK	OUT			31 (CS#)	15			G15	T12
66	AUDIO-SDTI	OUT			59	50		FLASH-RESET#	H14	M10
45	AUDIO-SDTO	IN			38 (DOUT/BSY	18			T11	K5
13	CLK	OUT			88 (GCK)	42			D6	F14
20	ETHER-AEN/PSEN#	OUT			85				A3	E14
42	ETHER-BHE#	OUT							T10	J3
64	ETHER-CLK	IN							C9 (GCK)	R9 (GCK)
9	ETHER-CS#	OUT			77				C6	G13
79	ETHER-IRQ	IN	BAR6		51	46	PP-D5	FLASH-A13	D9	L15
48	ETHER-RDY/DTACK	IN							N11	M2
23	I2C-SCL	OUT			86				P5	F5
24	I2C-SDA	IN/OUT			87				T4	D2
7	IDE-CS0#	OUT			79				B6	G15
8	IDE-CS1#	OUT			80				E7	G14
43	IDE-DMACK#	OUT							R10	K1
49	IDE-DMARQ	IN							T13	L4
44	IDE-IORDY	IN							P10	L2
3	IDE-IRQ	IN	BAR8		64	52	DIPSW1B	FLASH-A15	B7	H15
57	PB-A0	OUT	BAR1	PB2	40	1	PP-S3	FLASH-A0	P13	L5
56	PB-A1	OUT	BAR2	PB3	29	64	PP-S4	FLASH-A1	N12	N2
51	PB-A2	OUT	BAR3	PB4	28	63	PP-S5	FLASH-A2	R13	M3
50	PB-A3	OUT	BAR4		27	62		FLASH-A3	P12	N1
70	PB-A4	OUT	BAR5		74	61		FLASH-A4	F16	T13
71	PB-D0	IN/OUT		DIPSW1	39 (D0)	2	LED-S1	FLASH-D0	F14	P12
40	PB-D1	IN/OUT		DIPSW2	44 (D1)	4	LED-DP	FLASH-D1	P9	J1
39	PB-D2	IN/OUT		DIPSW3	46 (D2)	5	LED-S4	FLASH-D2	R9	H1
38	PB-D3	IN/OUT		DIPSW4	49 (D3)	6	LED-S6	FLASH-D3	T9	H3
35	PB-D4	IN/OUT		DIPSW5	57 (D4)	7	LED-S5	FLASH-D4	T7	G2
80	PB-D5	IN/OUT		DIPSW6	60 (D5)	8	LED-S3	FLASH-D5	B9	K15
81	PB-D6	IN/OUT		DIPSW7	62 (D6)	9	LED-S2	FLASH-D6	A9	K16
10	PB-D7	IN/OUT		DIPSW8	67 (D7)	10	LED-S0	FLASH-D7	A5	F15
27	PB-D8	IN/OUT	LED2-A		12		VGA-RED0		M7	E2
28	PB-D9	IN/OUT	LED2-B		13		VGA-RED1		R6	E1
29	PB-D10	IN/OUT	LED2-C		19		VGA-GREEN0		N7	F3
32	PB-D11	IN/OUT	LED2-D		20		VGA-GREEN1		P7	F2
33	PB-D12	IN/OUT	LED2-E		21		VGA-BLUE0		R7	G4
34	PB-D13	IN/OUT	LED2-F		22		VGA-BLUE1		T14	G3
36	PB-D14	IN/OUT	LED2-G		23		VGA-HSYNC#		P8	G1
37	PB-D15	IN/OUT	LED2-DP	PB1	26		VGA-VSYNC#		T8	H4
61	PB-RD#	OUT			43	12	PP-D7	FLASH-OE#	P16	P2
62	PB-WR#	OUT			58	49	PP-D6	FLASH-WE#	L12	R1
55	PROG#				69 (PROG#)	39			P15 (PROG#)	B3 (PROG#)
21	RESET_TRIGGER#	IN/OUT			111 (M1)				B3	D15
25	RS232-CTS	IN			93		PUSHB	PS2-DATA	R5	D1
31	RS232-RD	IN			15 (GCK)				T6	G5
26	RS232-RTS	OUT			94			PS2-CLK	P6	F4
41	RS232-TD	OUT			68 (INIT#)	38			N9	J2

Connections Between the XST-3.0 Board and the Various XSA Boards										
XStend Board					XSA-50 and XSA-100				XSA-200	XSA-3S1000
Proto. Pin	Net Name	Direction	LEDs	Switches	FPGA Pin	CPLD Pin	Misc. Functions		FPGA Pin	FPGA Pin
18	SLOT1-CS#	OUT			83				B4	E15
84	SLOT1-IRQ	IN	BAR9		63	51	DIPSW1C	FLASH-A16	D8	J16
19	SLOT2-CS#	OUT			84				E6	D16
83	SLOT2-IRQ	IN	BAR10		56	48	DIPSW1D	FLASH-A17	C8	J14
16	TCK				2 (TCK)	13			C4 (TCK)	C14 (TCK)
15	TDI				32 (TDI)	15			A15 (TDI)	R3 (TDI)
30	TDO				34 (TDO)	19			B14 (TDO)	T3 (TDO)
17	TMS				142 (TMS)	18			D3 (TMS)	P9 (TMS)
47	USB-CLK	IN							R12	M1
82	USB-IRQ#	IN	BAR7		54	47	DIPSW1A	FLASH-A14	A8	J13
46	USB-SUSPEND	IN							T12	L3
72	VIDIN-AVID	IN							F12	
1	VIDIN-CLK	IN			18 (GCK)				A7	H16
76	VIDIN-FID	IN							E10	
74	VIDIN-HSYNC	IN							E11	
63	VIDIN-IRQ	IN							M14	
75	VIDIN-VSYNC	IN							D11	
4	VIDIN-Y0	IN	LED1-A		65	56	PP-D4	FLASH-A12	C7	H14
59	VIDIN-Y1	IN	LED1-B		47	43	PP-D3	FLASH-A11	R16	M4
58	VIDIN-Y2	IN	LED1-C		42	57	PP-D2	FLASH-A10	T15	P1
60	VIDIN-Y3	IN	LED1-D		48	44	PP-D1	FLASH-A9	M13	N3
78	VIDIN-Y4	IN	LED1-E		50	45	PP-D0	FLASH-A8	A10	M15
5	VIDIN-Y5	IN	LED1-F		66	58		FLASH-A7	A6	H13
6	VIDIN-Y6	IN	LED1-G		76	59		FLASH-A6	D7	G16
77	VIDIN-Y7	IN	LED1-DP		75	60		FLASH-A5	B10	N15
11									B8 (GCK)	P8 (GCK)
12					106 (M2)				B5	G12
14					109 (M0)	36			A4	E16
53					72 (DONE)	40			M11	
65					41	11		FLASH-CE#		
73					37 (CCLK)	16			B16	

B

XStend Schematics

The following pages show the detailed schematics for the XStend Board.



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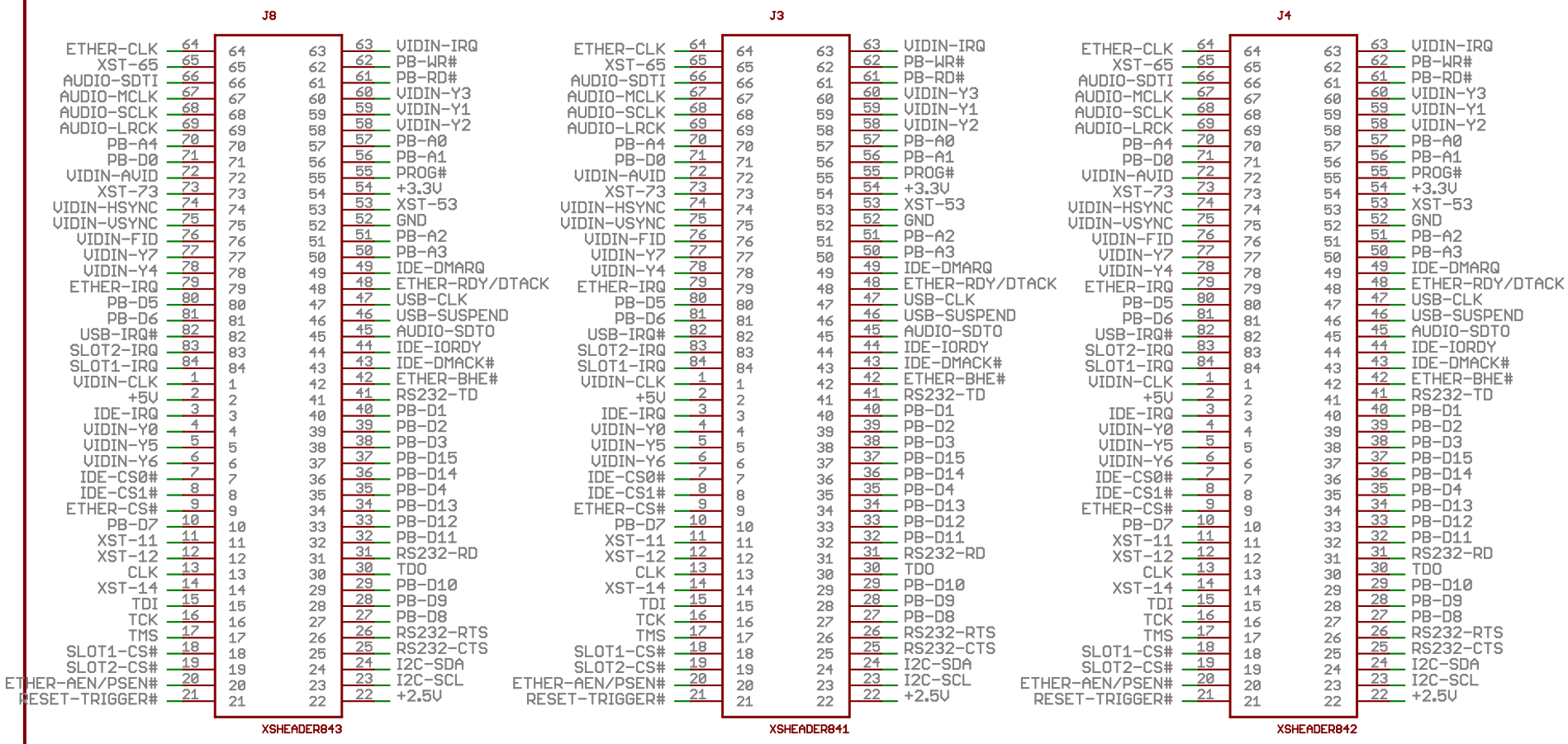

XSA Mounting Socket and Proto. Area Connector

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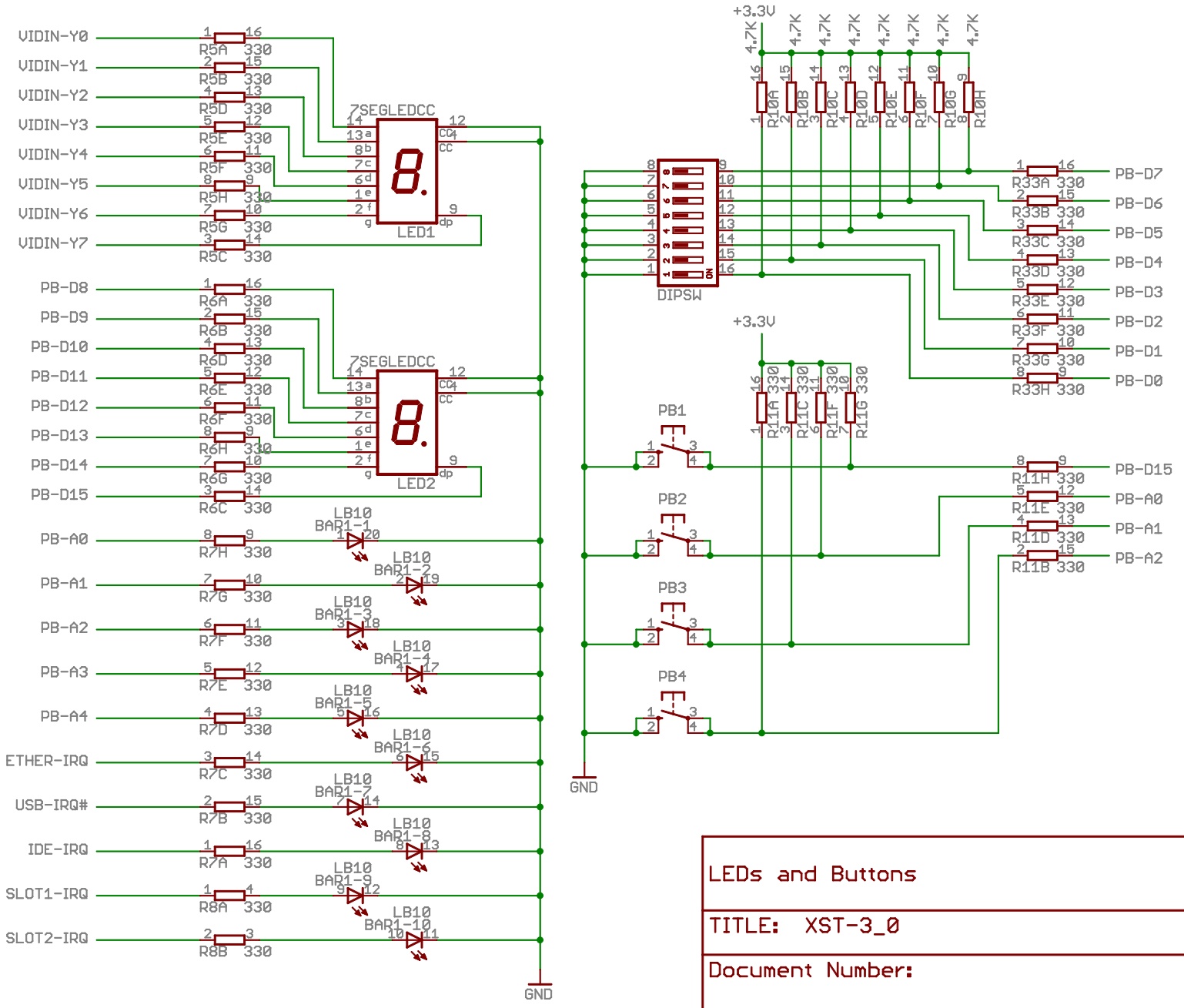

LEDs and Buttons		
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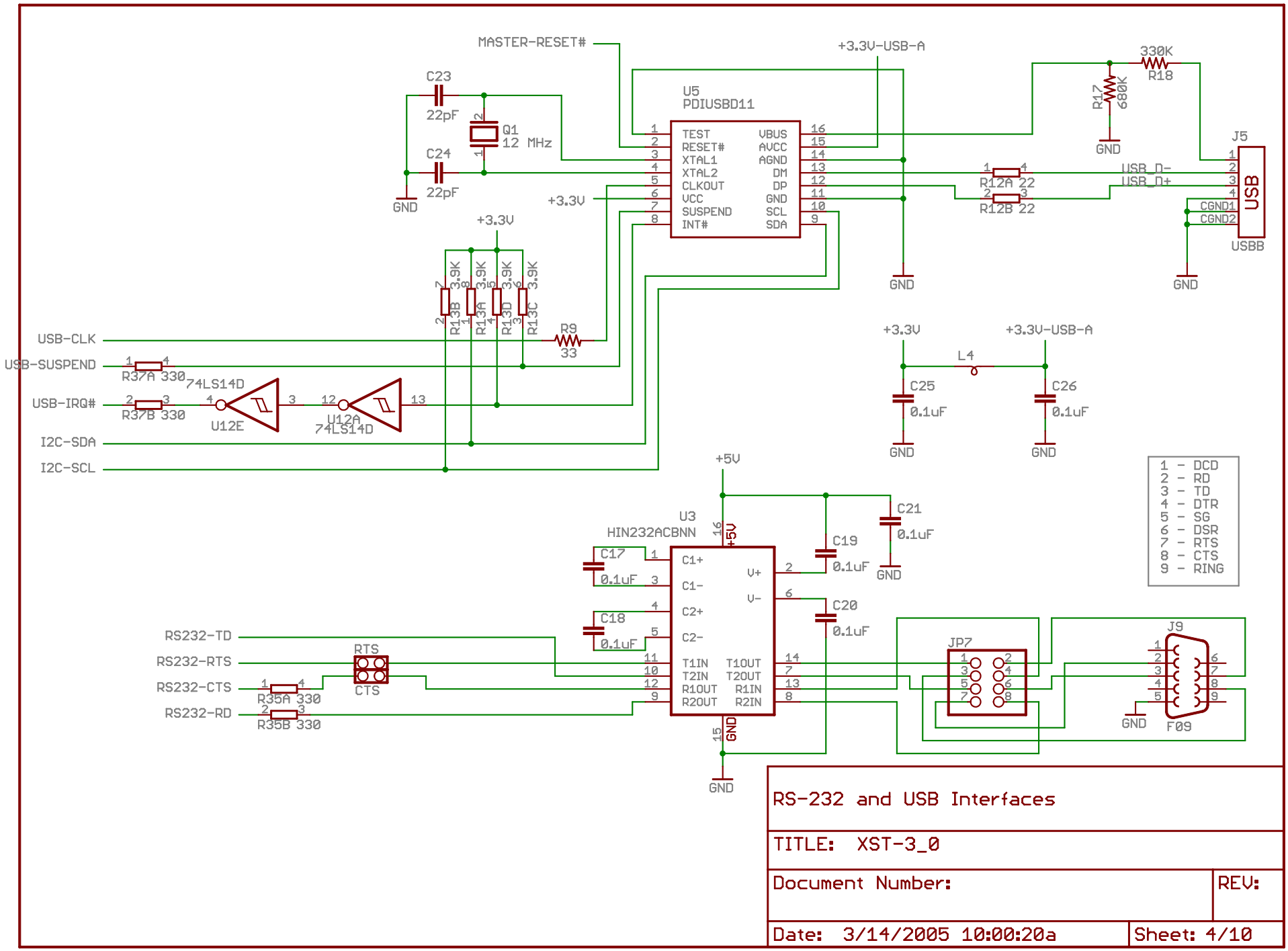
MASTER-RESET#
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330K
R18
R17
680K
C23
22pF
Q1
12 MHz
C24
22pF
U5
PDIUSBD11
TEST
RESET#
XTAL1
XTAL2
CLKOUT
VCC
SUSPEND
INT#
VBUS
AVCC
AGND
DM
DP
GND
SCL
SDA
GND
+3.3V
+3.3V
R12A 22
R12B 22
USB_D-
USB_D+
J5
USB
CGND1
CGND2
USBB
GND
GND
R13B 3.9K
R13A 3.9K
R13D 3.9K
R13C 3.9K
R9
33
USB-CLK
USB-SUSPEND
USB-IRQ#
I2C-SDA
I2C-SCL
R37A 330
R37B 330
74LS14D
U12E
U12A
74LS14D
+3.3V
+3.3V-USB-A
L4
C25
0.1uF
C26
0.1uF
GND
GND
1 - DCD
2 - RD
3 - TD
4 - DTR
5 - SG
6 - DSR
7 - RTS
8 - CTS
9 - RING
+5V
U3
HIN232ACBNN
C17
0.1uF
C18
0.1uF
C19
0.1uF
C20
0.1uF
C21
0.1uF
C1+
C1-
C2+
C2-
V+
V-
T1IN
T2IN
R1OUT
R2OUT
T1OUT
T2OUT
R1IN
R2IN
GND
GND
RS232-TD
RS232-RTS
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RTS
CTS
R35A 330
R35B 330
JP7
J9
F09
GND
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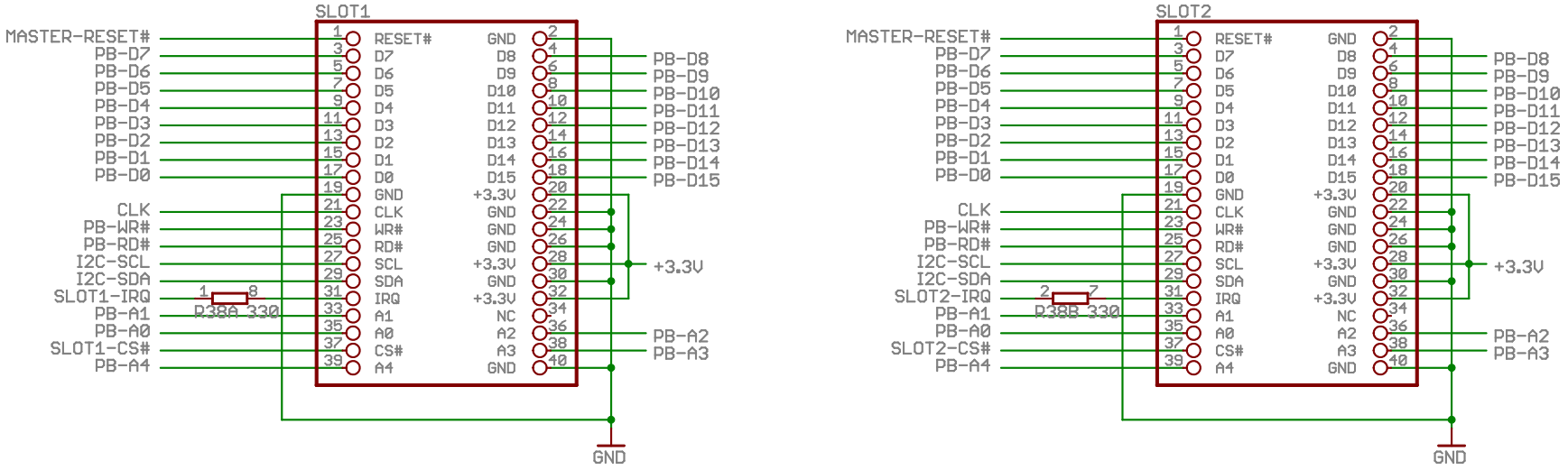

Daughterboard Slots		
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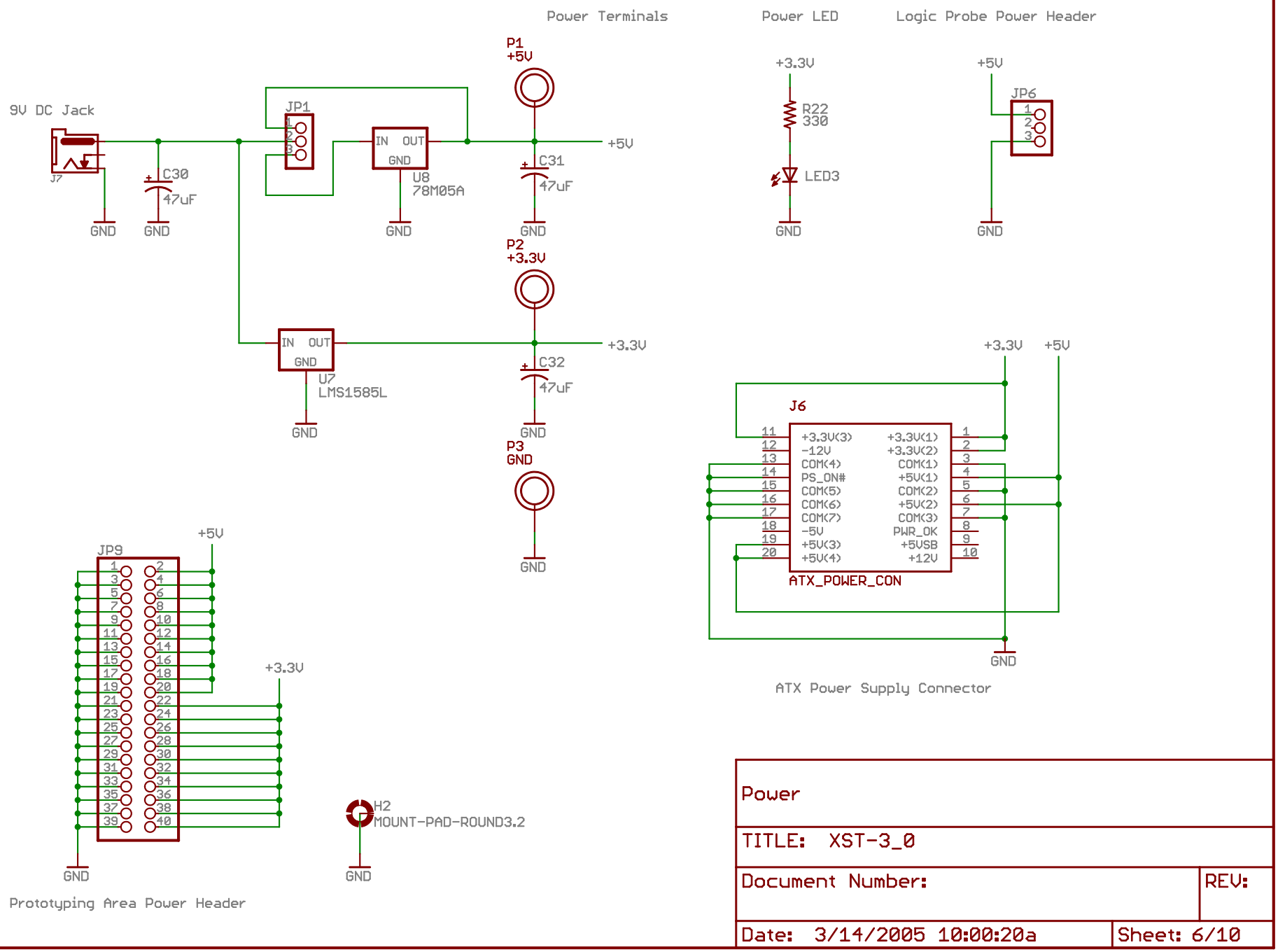
Power Terminals
Power LED
Logic Probe Power Header
9V DC Jack
J7
JP1
C30
47uF
GND
U8
78M05A
IN
OUT
C31
47uF
P1
+5V
+5V
R22
330
LED3
+3.3V
JP6
P2
+3.3V
U7
LMS1585L
C32
47uF
P3
GND
J6
+3.3V(3)
-12V
COM(4)
PS_ON#
COM(5)
COM(6)
COM(7)
-5V
+5V(3)
+5V(4)
+3.3V(1)
+3.3V(2)
COM(1)
+5V(1)
COM(2)
+5V(2)
COM(3)
PWR_OK
+5VSB
+12V
ATX_POWER_CON
ATX Power Supply Connector
JP9
Prototyping Area Power Header
H2
MOUNT-PAD-ROUND3.2
Power
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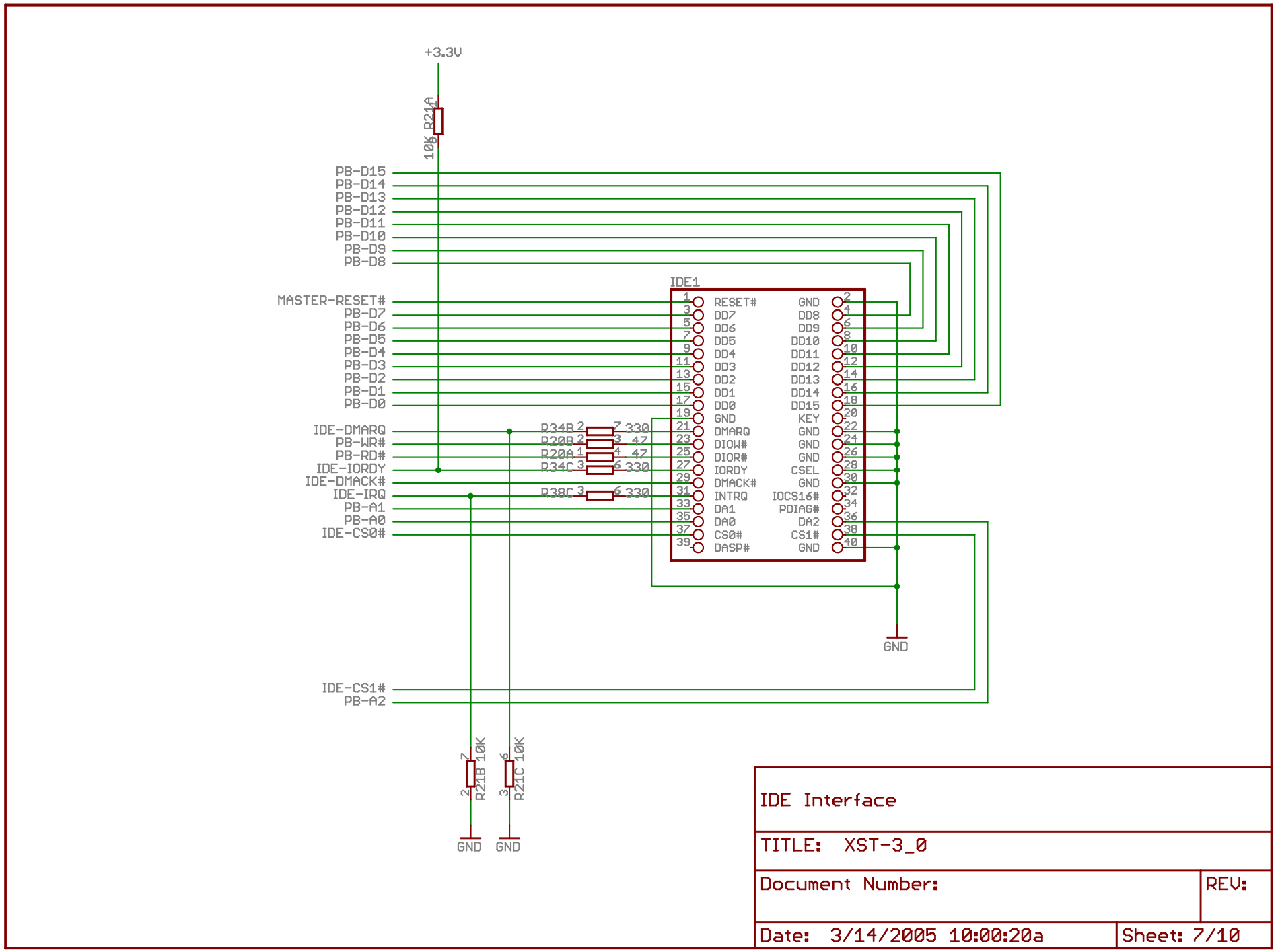
+3.3V
10K R21A
PB-D15
PB-D14
PB-D13
PB-D12
PB-D11
PB-D10
PB-D9
PB-D8
MASTER-RESET#
PB-D7
PB-D6
PB-D5
PB-D4
PB-D3
PB-D2
PB-D1
PB-D0
IDE-DMARQ
PB-WR#
PB-RD#
IDE-IORDY
IDE-DMACK#
IDE-IRQ
PB-A1
PB-A0
IDE-CS0#
IDE-CS1#
PB-A2
IDE1
RESET# DD7 DD6 DD5 DD4 DD3 DD2 DD1 DD0 GND DMARQ DIOW# DIOR# IORDY DMACK# INTRQ DA1 DA0 CS0# DASP#
GND DD8 DD9 DD10 DD11 DD12 DD13 DD14 DD15 KEY GND GND GND CSEL GND IOCS16# PDIAG# DA2 CS1# GND
R34B 330
R20B 47
R20A 47
R34C 330
R38C 330
R21B 10K
R21C 10K
GND
GND
GND
IDE Interface
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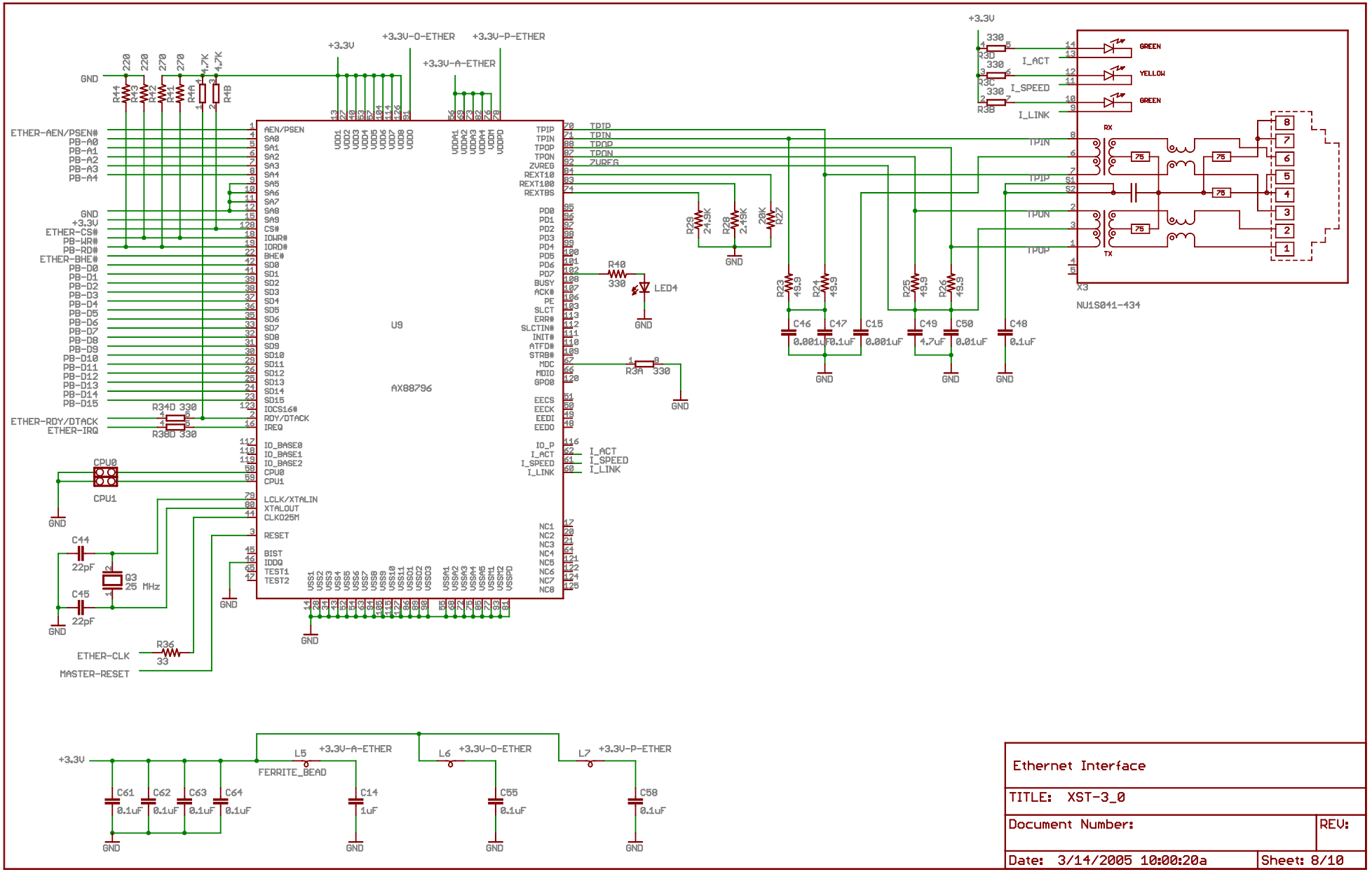

Ethernet Interface	
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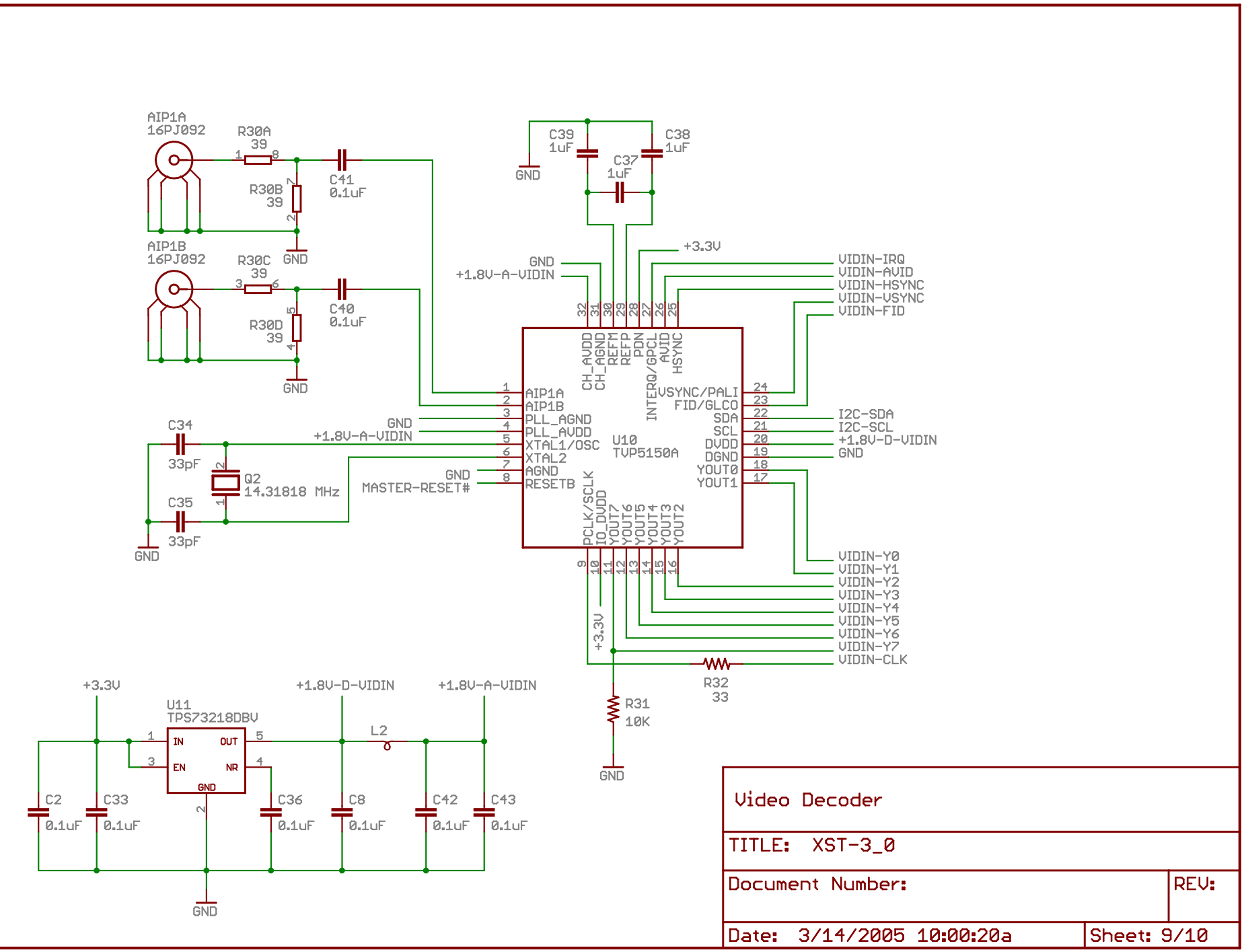
AIP1A
16PJ092
R30A
39
R30B
39
C41
0.1uF
AIP1B
16PJ092
R30C
39
R30D
39
C40
0.1uF
GND
C39
1uF
C38
1uF
C37
1uF
+3.3V
GND
+1.8V-A-VIDIN
VIDIN-IRQ
VIDIN-AVID
VIDIN-HSYNC
VIDIN-VSYNC
VIDIN-FID
CH_AVDD
CH_AGND
REFM
REFP
PDN
INTERQ/GPCL
AVID
HSYNC
AIP1A
AIP1B
PLL_AGND
PLL_AVDD
XTAL1/OSC
XTAL2
AGND
RESETB
U10
TVP5150A
VSYNC/PALI
FID/GLCO
SDA
SCL
DVDD
DGND
YOUT0
YOUT1
I2C-SDA
I2C-SCL
+1.8V-D-VIDIN
GND
C34
33pF
C35
33pF
Q2
14.31818 MHz
GND
+1.8V-A-VIDIN
GND
MASTER-RESET#
PCLK/SCLK
IO_DVDD
YOUT7
YOUT6
YOUT5
YOUT4
YOUT3
YOUT2
VIDIN-Y0
VIDIN-Y1
VIDIN-Y2
VIDIN-Y3
VIDIN-Y4
VIDIN-Y5
VIDIN-Y6
VIDIN-Y7
VIDIN-CLK
+3.3V
R32
33
R31
10K
GND
+3.3V
U11
TPS73218DBV
IN
OUT
EN
NR
GND
L2
+1.8V-D-VIDIN
+1.8V-A-VIDIN
C2
0.1uF
C33
0.1uF
C36
0.1uF
C8
0.1uF
C42
0.1uF
C43
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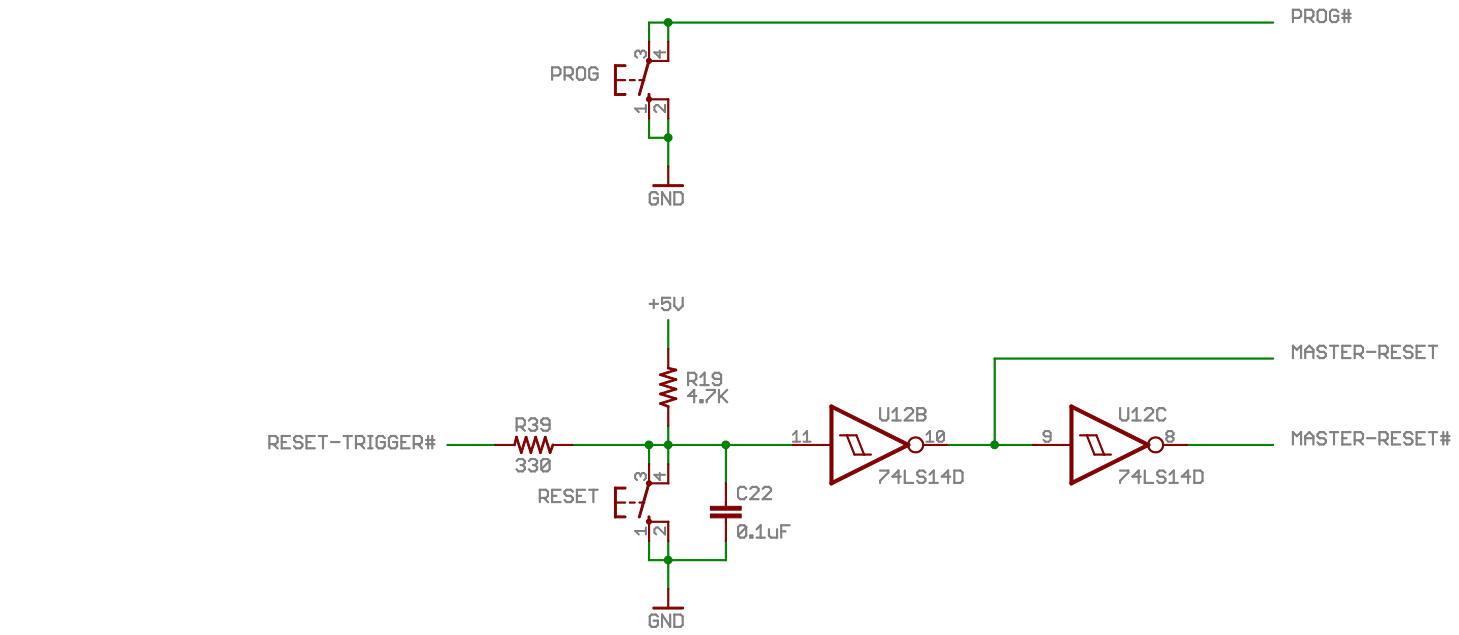

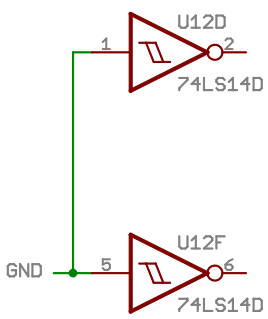

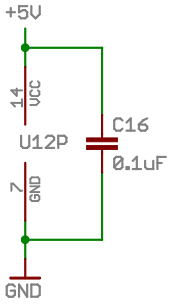

Reset Circuitry	
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