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XStend Board V2.0 Manual

How to install and use your new XStend Board

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Preliminaries

Getting Help!

Here are some places to get help if you encounter problems:

- If you can't get the XStend Board hardware to work, send an e-mail message describing your problem to help@xess.com or submit a problem report at http://www.xess.com/help.html. Our web site also has
  - answers to frequently-asked-questions,
  - example designs for the XS Boards,
  - application notes,
  - a place to sign-up for our email forum where you can post questions to other XS Board users.

Take notice!!

- The XStend Board V2.0 is not compatible with the XS95, XS40 or XSTE5 Boards! Do not plug XS95, XS40 or XSTE5 Boards into the XStend Board V2.0!
- If you are connecting a 9VDC power supply to your XStend Board, please make sure the center terminal of the plug is positive and the outer sleeve is negative!

Packing List

Here is what you should have received in your package:

- an XStend Board;
- an XSTOOLs CDROM with software utilities and documentation for using the XStend Board.

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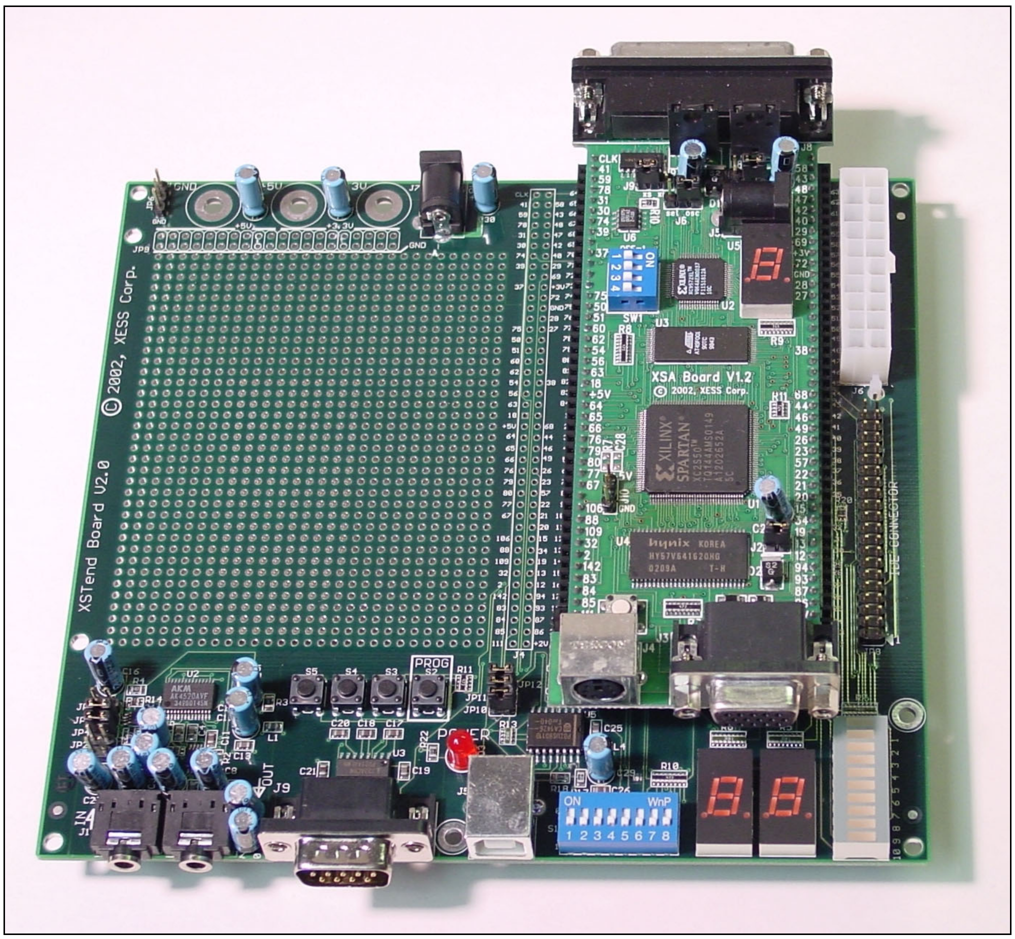
Installation

Inserting the XSA Board into an XStend Board

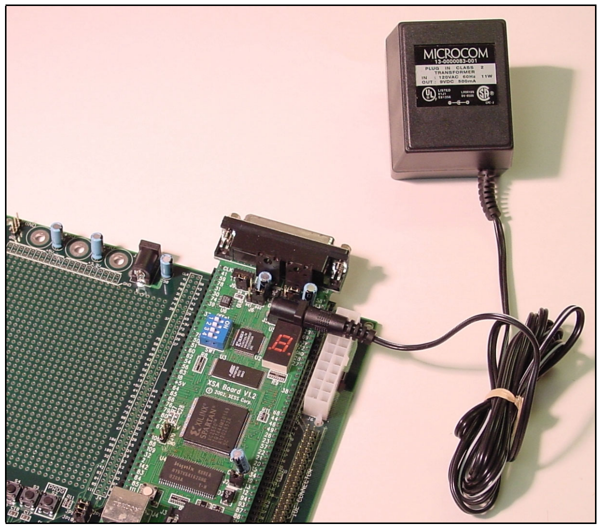
The XSA Board is inserted into the XStend Board as shown below. The XSA Board is inserted into the inner-most columns of the socket strips. **Orient the parallel port, VGA port and PS/2 port connectors on the XSA Board as indicated on the XStend Board!!**



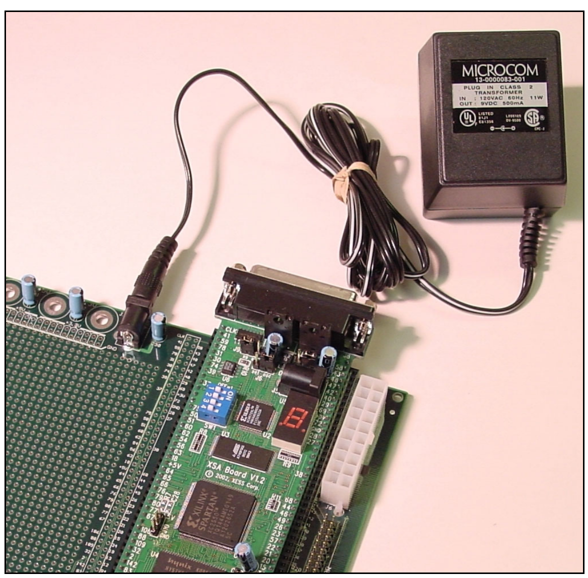
Applying Power to Your XStend Board

You can supply power to your XStend Board in four ways. ***Do not apply power from more than one source at a time!!***

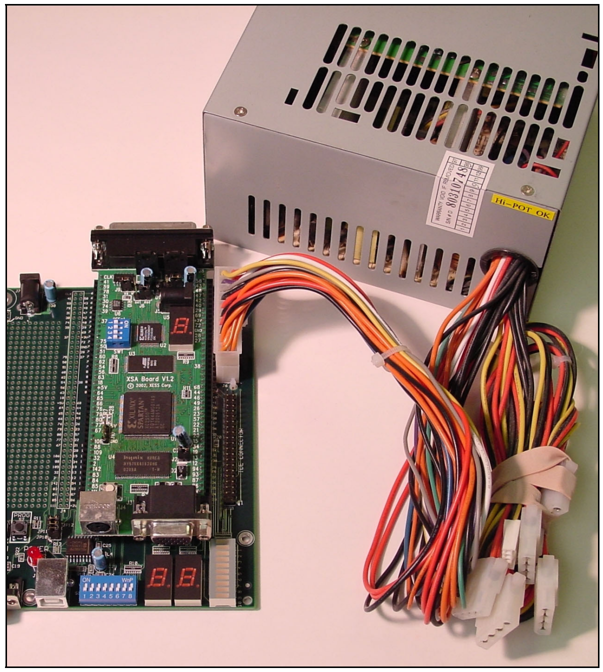
You can attach a 9V DC power supply to the XSA Board and the XStend Board will draw its power through the XSA Board prototyping header as shown below. (The power supply should have a 2.1 mm female, center-positive plug and be capable of delivering at least 500 mA.)



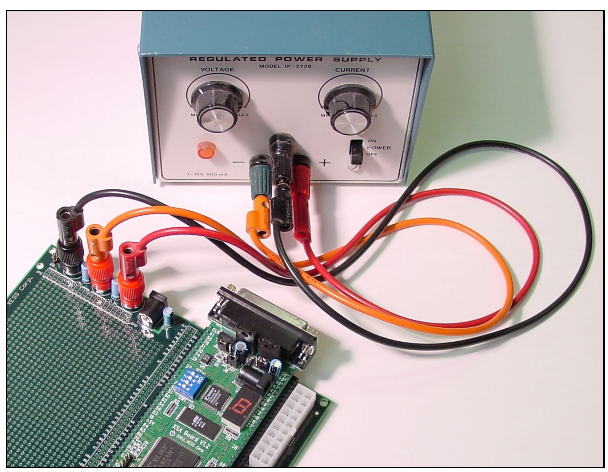
Or you can attach the 9V DC power supply directly to jack J7 on the XStend Board. Now the XSA Board will draw its power from the XStend Board.



You can also attach a standard ATX PC power supply to the XStend Board through connector J6.



Finally, you can power the XStend Board from a dual 5V / 3.3V power supply directly to the binding posts on the XStend Board.



Making Connections to Your XSA and XStend Boards

You can make the same connections to your XSA Board whether it is inserted into the XStend Board or used stand-alone. A 6' DB25 male-to-male cable attaches from the parallel port on the PC to the female DB-25 connector (J8) at the top on the XSA Board. You can connect a VGA monitor to the 15-pin connector (J3) at the bottom of your XSA Board. And you can accept inputs from a keyboard or mouse by connecting it to the PS/2 connector (J4) at the bottom of your XSA Board.

The XStend Board offers some additional connection opportunities. You can connect the peripheral end of a USB 1.1 cable to the USB port (J5) on the XStend Board while the host end attaches to a PC USB port. You can enable serial communications by attaching a 9-pin RS-232 null-modem cable between the DB9 connector (J9) on the XStend Board and a serial port on a PC. You can capture audio output from a CD player or a microphone by attaching them to the 3.5mm stereo input jack (J1) on the XStend Board, while audio can be sent to a pair of headphones through the stereo output jack (J2).

Setting the Jumpers on Your XStend Board

The default jumper settings shown in Table 1 configure your XStend Board for use in a logic design environment. You will need to change the jumper settings only if you are:

- manually reseting the audio codec circuit,
- accepting audio signals from a low-amplitude source (e.g., a passive microphone),
- not using the USB interface.

• Table 1: Jumper settings for XSA Boards.

Jumper	Setting	Purpose
JP1	Off (default)	Removing this shunt allows the audio codec to process stereo audio signals.
	On	Placing a shunt on this jumper resets the audio codec and halts any input or output of stereo audio signals.
JP2	Off (default)	Removing this shunt interrupts power to a passive microphone attached to the left stereo input channel.
	On	Placing a shunt on this jumper provides power to a passive microphone attached to the left stereo input channel.
JP3	Off (default)	Removing this shunt interrupts power to a passive microphone attached to the right stereo input channel.
	On	Placing a shunt on this jumper provides power to a passive microphone attached to the right stereo input channel.
JP4	Off	Removing this shunt sets the gain on the left stereo input channel to 48.
	On (default)	Placing a shunt on this jumper sets the gain on the left stereo input channel. to 1.
JP5	Off	Removing this shunt sets the gain on the right stereo input channel to 48.
	On (default)	Placing a shunt on this jumper sets the gain on the right stereo input channel. to 1.
JP10	Off	Removing this shunt disconnects the XSA Board from the I^2C data signal of the USB interface.
	On (default)	Placing a shunt on this jumper connects the XSA Board to the I^2C data signal of the USB interface.
JP11	Off	Removing this shunt disconnects the XSA Board from the I^2C clock signal of the USB interface.
	On (default)	Placing a shunt on this jumper connects the XSA Board to the I^2C clock signal of the USB interface.
JP12	Off	Removing this shunt disconnects the XSA Board from the clock output of the USB interface.
	On (default)	Placing a shunt on this jumper connects the XSA Board to the clock output of the USB interface.

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Programmer's Models

This section describes the various sections of the XStend Board and shows how the prototyping header pins of the XSA Board are connected to the XStend Board circuitry. Please refer to the complete schematics and pin list at the end of this document if you need more details.

XStend Board Capabilities

The XSA Boards offer a flexible, low-cost method of prototyping FPGA designs. However, their small physical size limits the amount of support circuitry they can hold. The XStend Board removes this limitation by providing additional support circuitry that the XSA Boards can access through their prototyping header interfaces.

The XStend Board contains resources that extend the range of applications of the XSA Boards into these new areas:

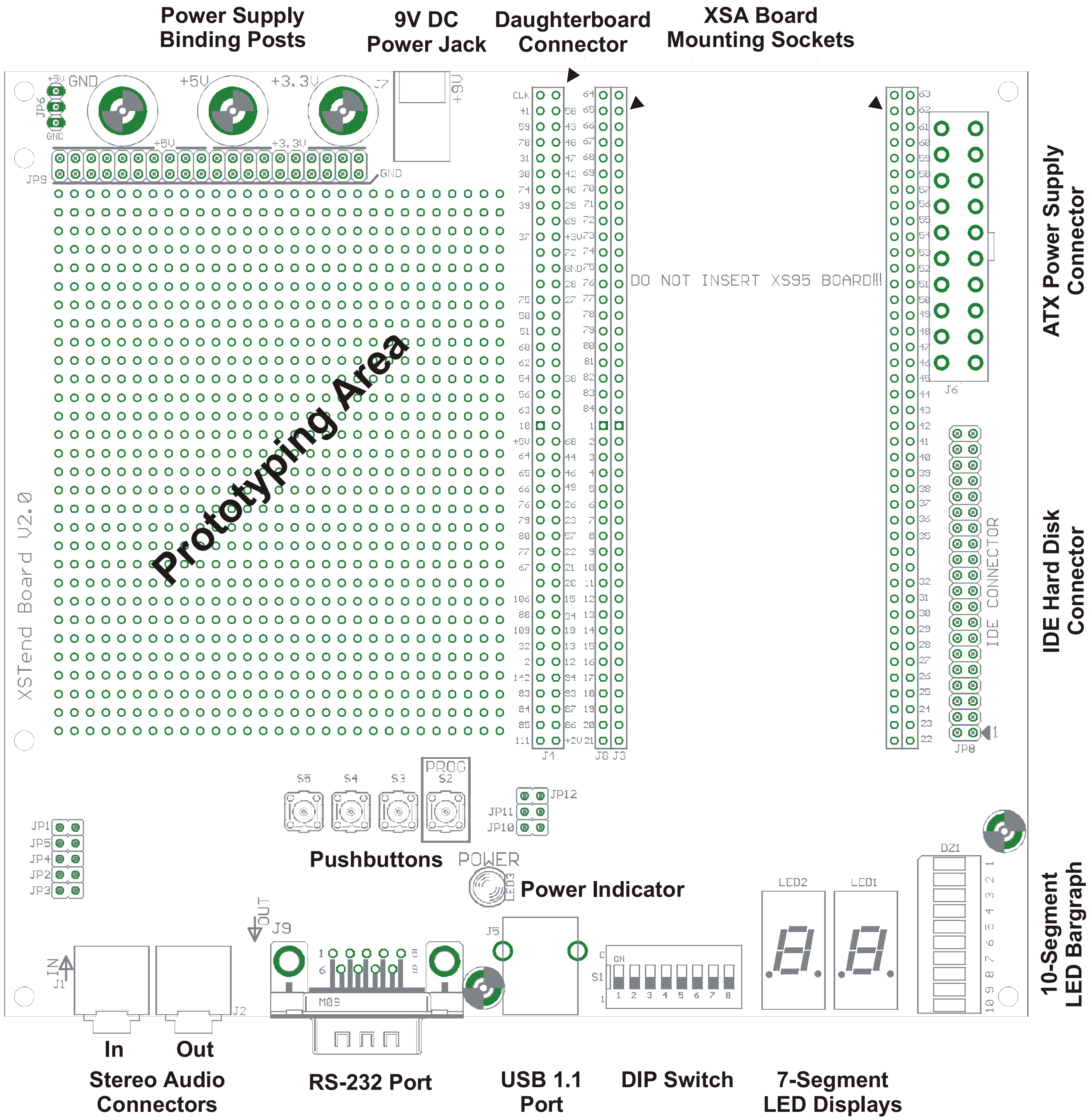
- The pushbuttons, DIP switches, LEDs, and prototyping area are useful for basic lab experiments.
- The static RAM can be used when the larger SDRAM on the XSA Board is overkill for a particular application.
- The stereo codec and dual-channel analog input/output circuitry are useful for processing of audio signals in combination with DSP circuits synthesized for the FPGA.
- The USB 1.1 interface lets the XSA Board appear as a low-speed or full-speed USB peripheral to a PC.
- The RS-232 interface is useful when the XSA Board needs to send information over a low-speed serial communication link.
- The IDE interface provides the XSA Board with access to a hard disk for data storage and retrieval.

XStend Board Components

The XStend Board extends the capabilities of the XSA Boards by providing:

- additional bargraph LED and LED digits;
- DIP switches and pushbuttons;
- an RS-232 port;
- a USB 1.1 peripheral interface;
- an additional 128 Kbytes of static RAM;
- an IDE interface to hard disks;
- a stereo audio codec with left/right input and output channels;
- mounting sockets for an XSA Board;
- a 42×2 header connector for add-on daughterboards (optional);
- a 2.75"×3.5" prototyping area with access to both the 3.3V or 5V supply.

These resources are shown in the simplified view of the XStend Board. Each of these resources will be described in the following sections.



• Figure 1: Simplified layout of the XStend Board.

LEDs

The XStend Board provides an XSA Board with a ten-segment bargraph LED and two more LED seven-segment displays. All of these LEDs are active-high meaning that an LED segment will glow when a high logic level is applied to it.

Listing 1 shows the connections from the FPGA on the XSA Board to the LEDs on the XStend Board expressed as UCF constraints (for the UCF syntax and usage tips, check out http://www.xilinx.com/techdocs/2449.htm).

- **Listing 1:** Connections between the XStend LEDs and the FPGA on the XSA Board.

```
net ledtwo<0>   loc=p47;  # rightmost 7-segment LED
net ledtwo<1>   loc=p40;
net ledtwo<2>   loc=p28;
net ledtwo<3>   loc=p29;
net ledtwo<4>   loc=p27;
net ledtwo<5>   loc=p42;
net ledtwo<6>   loc=p48;
net ledtwo<7>   loc=p38;
net ledone<0>   loc=p64;  # leftmost 7-segment LED
net ledone<1>   loc=p65;
net ledone<2>   loc=p76;
net ledone<3>   loc=p50;
net ledone<4>   loc=p51;
net ledone<5>   loc=p54;
net ledone<6>   loc=p56;
net ledone<7>   loc=p63;
net barled<1>   loc=p68;  # bargraph LED
net barled<2>   loc=p44;
net barled<3>   loc=p46;
net barled<4>   loc=p49;
net barled<5>   loc=p57;
net barled<6>   loc=p62;
net barled<7>   loc=p60;
net barled<8>   loc=p67;
net barled<9>   loc=p39;
net barled<10>  loc=p59;
```

DIP Switch and Pushbuttons

The XStend has a bank of eight DIP switches and three pushbuttons that are accessible by an XSA Board. (There is a fourth pushbutton labeled PROG, which is used to initiate the programming of the XSA Board. It is not intended to be a general-purpose input.)

When closed or ON, each DIP switch pulls the connected pin of the XS Board to ground. When the DIP switch is open or OFF, the pin is pulled high through a resistor. ***When not being used, the DIP switches should be left in the open or OFF configuration so the pins of the XSA Board are not tied to ground and can freely move between logic low and high levels.***

When pressed, each pushbutton pulls the connected pin of the XS Board to ground. Otherwise, the pin is pulled high through a resistor.

Listing 2 shows the connections from the FPGA on the XSA Board to the switches on the XStend Board expressed as UCF constraints.

- **Listing 2:** Connections between the XStend DIP/pushbutton switches and the FPGA on the XSA Board.

```
net pushsw<3>   loc=p78;  # pushbuttons
net pushsw<4>   loc=p26;
net pushsw<5>   loc=p23;
net dipsw<1>    loc=p30;  # DIP switches
net dipsw<2>    loc=p58;
net dipsw<3>    loc=p74;
net dipsw<4>    loc=p75;
net dipsw<5>    loc=p66;
net dipsw<6>    loc=p77;
net dipsw<7>    loc=p80;
net dipsw<8>    loc=p79;
```

RS-232 Port

The XStend Board has a 9-pin RS-232 port that provides the XSA Board with the transmit and receive serial data streams (TD and RD, respectively) as well as the flow control signals (RTS and CTS, respectively). The pin functions on the XStend Board RS-232 port are identical to those found on a PC serial port, so a null modem cable that swaps the TD/RD and CTS/RTS lines is needed if the XStend Board and PC are to communicate.

Listing 3 shows the connections from the FPGA on the XSA Board to the RS-232 port pisn on the XStend Board expressed as UCF constraints.

- **Listing 3:** Connections between the XStend RS-232 port and the FPGA on the XSA Board.

```
net td   loc=p83;  # RS232 TD port pin 3
net rd   loc=p60;  # RS232 RD port pin 2
net rts  loc=p80;  # RS232 RTS port pin 7
net cts  loc=p62;  # RS232 CTS port pin 8
```

USB 1.1 Interface

The XStend Board uses a USB-to-I^2C interface chip (Phillips part# PDIUSBD11) to provide the XSA Board with a USB communication link. The FPGA accesses registers on the chip via the serial clock and data lines of the I^2C link. By reading and writing these registers, the FPGA can act as a USB peripheral with the chip handling the low-level data transactions for the USB bus.

The USB interface chip also provides an interrupt signal to alert the FPGA when USB tranactions need to be processed. In addition, a SUSPEND signal is also output from the chip to alert the FPGA when the USB bus loses power or otherwise ceases operations. Finally, a clock output from the chip is made available to the external clock input of the programmable oscillator on the XSA Board. The frequency of this clock is 48 MHz / (N+1) where N is a value loaded into a register on the chip through the I^2C interface.

Listing 4 shows the connections from the FPGA on the XSA Board to the USB interface chip on the XStend Board expressed as UCF constraints.

• **Listing 4:** Connections between the XStend USB interface chip and the FPGA on the XSA Board.

```
net sda   loc=p85;  # I2C data signal
net scl   loc=p84;  # I2C clock signal
net susp  loc=p29;  # SUSPEND signal
net intr  loc=p28;  # INTERRUPT signal
```

SRAM

The XStend Board gives the XSA Board access to a 128 KByte SRAM (Alliance part# AS7C1024-15TJC).

Listing 5 shows the connections from the XSA Board to the SRAM on the XStend Board (expressed as UCF constraints):

• **Listing 5:** Connections between the XStend SRAM and the FPGA on the XSA Board.

```
net ceb   loc=p79;  # chip-enable (active-low)
net oeb   loc=p43;  # output-enable (active-low)
net web   loc=p58;  # write-enable (active-low)
net a<0>  loc=p27;  # address lines
net a<1>  loc=p38;
net a<2>  loc=p66;
net a<3>  loc=p65;
net a<4>  loc=p64;
net a<5>  loc=p63;
net a<6>  loc=p56;
net a<7>  loc=p54;
net a<8>  loc=p42;
net a<9>  loc=p40;
net a<10> loc=p28;
net a<11> loc=p29;
net a<12> loc=p51;
net a<13> loc=p47;
net a<14> loc=p50;
net a<15> loc=p48;
net a<16> loc=p39;
net d<0>  loc=p60;  # data lines
net d<1>  loc=p62;
net d<2>  loc=p67;
net d<3>  loc=p57;
net d<4>  loc=p49;
net d<5>  loc=p46;
net d<6>  loc=p44;
net d<7>  loc=p68;
```

IDE Interface

The XStend Board provides the XSA Board with access to a hard disk through the IDE interface connector. The FPGA stores and retrieves data from the disk by reading and writing registers on the disk through the IDE interface. These registers are accessed using the read and write strobes in combination with the register bank select lines, the three-bit register address bus and the sixteen-bit IDE data bus.

In addition to polled access, the IDE interface also allows DMA access using the DMA request and acknowledge signals along with the I/O ready signal.

Listing 6 shows the connections from the FPGA on the XSA Board to the IDE interface chip on the XStend Board expressed as UCF constraints.

• **Listing 6:** Connections between the XStend IDE interface and the FPGA on the XSA Board.

```
net ide_resetb  loc=p31;  # reset
net ide_dmarq   loc=p27;  # DMA request
net ide_dmackb  loc=p38;  # DMA acknowledge
net ide_intrq   loc=p40;  # interrupt
net ide_iordy   loc=p39;  # I/O ready
net ide_diorb   loc=p86;  # read strobe
net ide_diowb   loc=p87;  # write strobe
net ide_cs0b    loc=p54;  # register bank select 0
net ide_cs1b    loc=p56;  # register bank select 1
net ide_da<0>   loc=p64;  # register address lines
net ide_da<1>   loc=p66;
net ide_da<2>   loc=p63;
net ide_d<0>    loc=p68;  # data I/O lines
net ide_d<1>    loc=p44;
net ide_d<2>    loc=p46;
net ide_d<3>    loc=p49;
net ide_d<4>    loc=p57;
net ide_d<5>    loc=p62;
net ide_d<6>    loc=p60;
net ide_d<7>    loc=p67;
net ide_d<8>    loc=p42;
net ide_d<9>    loc=p43;
net ide_d<10>   loc=p47;
net ide_d<11>   loc=p48;
net ide_d<12>   loc=p50;
net ide_d<13>   loc=p51;
net ide_d<14>   loc=p58;
net ide_d<15>   loc=p65;
```

Stereo Audio Codec

The XStend Board has a stereo audio codec (AKM part# AK4520AVF) that accepts two analog input channels, digitizes the analog values, and sends the digital values to the XSA Board as a serial bit stream. The codec also accepts a serial bit stream from the XSA Board and converts it into two analog output signals that exit the XStend Board.

Listing 7 shows the connections from the FPGA on the XSA Board to the codec interface on the XStend Board (expressed as UCF constraints):

• **Listing 7:** Connections between the XStend stereo codec and the FPGA on the XSA Board.

```
net mclk        loc=p77;  # master clock to codec
net lrck        loc=p59;  # left/right codec chaneel select
net sclk        loc=p75;  # serial data clock
```

```
net sdin        loc=p74;  # serial data stream to codec
net sdout       loc=p76;  # serail data stream from codec
```

The analog stereo input and output signals enter and exit the XStend Board through the 3.5mm jacks J1 and J2, respectively. The output of an audio CD player can be input through J1 and a set of small stereo headphones can be connected to J2 for listening to the processed output. In addition, a passive microphone can be connected to J1 by placing shunts on jumpers JP2 and JP3 and removing shunts from JP4 and JP5.

XSA Board Mounting Sockets

The XSA Board is mounted using the inner rows of the double-row sockets on the XStend Board. These sockets connect the prototyping header of the XSA Board to the components of the XStend Board.

In addition, the outer rows of each socket provide access points for probing the signals that go through the sockets. Each hole in the outer rows is electrically connected to the horizontally adjacent hole on the inner rows. Small wires (22-gauge or less) can be inserted in the holes on the outer rows and logic or oscilloscope probes can be attached to monitor the signals going through the mounting socket.

Daughterboard Connector

Daughterboards with specialized circuitry can be connected to the XStend board through connector J4. This 42×2 connector brings all the I/O and VCC/GND from the XSA Board to the daughterboard.

Prototyping Area

The XStend Board has a prototyping area consisting of component through-holes on an 0.1"×0.1" grid. Components in this area can access to the +5V, +3.3V and signal ground by making connections to the appropriate pins on the JP9 header.

Connections from the XSA Board to the prototyping area are made through the daughterboard header. Each pin on J4 is explicitly labeled with the corresponding number of the FPGA pin it connects to on the XSA Board. For example, the pin at the bottom-left of J4 on the XStend Board is connected to pin 111 of the FPGA on the XSA Board.

Interactions Between XSA Board and XStend Board Components

Many of the FPGA pins on the XSA Board are connected to two or more components on the XSA and/or XStend Board. This causes interactions that may make it difficult or impossible to use these components in the same application. This section will provide an overview discussion of some of the possible interactions between the components. These discussions are overly pessimistic in terms of what components cannot be used together in a single application, so advanced users are encouraged to check the list of pin assignments in Appendix A for more details.

XSA Pushbutton Interactions

The pushbutton on the XSA Board connects to the same FPGA pin as the data pin of the XSA Board's PS/2 port. These components cannot be used simultaneously.

XSA VGA Port Interactions

The horizontal and vertical sync signals of the XSA Board use the same FPGA pins as two of the pushbuttons on the XStend Board (SW3 and SW4). These components cannot be used simultaneously.

XSA DIP Switches

The DIP switch on the XSA Board shares FPGA pins with the XSA Board Flash RAM and the XStend Board SRAM chip, seven-segment LED (LED1) and the IDE interface. Therefore, the XSA Board DIP switches should be left in the OFF (OPEN) position if these other components are being used.

XSA Flash RAM

The Flash RAM on the XSA Board shares FPGA pins with the XSA Board DIP switch, seven-segment LED and CPLD parallel port interface, and with the XStend Board SRAM, both seven-segment LEDs, bargraph LED, stereo audio codec, DIP switch, USB port and IDE interface.

The Flash RAM and SRAM can be deselected using their respective chip-select signals, so these components can be used simultaneously in an application. The IDE interface can also be used at the same time as these other two components by activating its read or write control signal only when the Flash RAM and SRAM are deselected.

The codec, DIP switches (on both the XSA and XStend Boards), LEDs (on both the XSA and XStend Boards) and USB port do not have chip-selects. Therefore, these components cannot be used in applications where the Flash RAM is needed.

The default parallel port interface programmed into the XSA Board CPLD will disable outputs that interfere would interfere with the operations of the Flash RAM. Therefore, it can be used without modification in applications that employ the Flash RAM.

XSA Seven-Segment LED

The seven-segment LED on the XSA Board shares FPGA pins with the XSA Board Flash RAM and the XStend Board SRAM, bargraph LED, RS-232 port and IDE interface. Therefore, these components cannot be used in applications where the seven-segment LED on the XSA Board is needed.

XSA SDRAM

The synchronous DRAM chip on the XSA Board does not share any FPGA pins with any other components. Therefore, any application can use the SDRAM regardless of the other components that are to be used.

XStend Codec

The stereo audio codec on the XStend Board shares FPGA pins with the XSA Board Flash RAM and the XStend Board bargraph LED, seven-segment LED (LED1), and DIP switch. Therefore, these components cannot be used in applications where the codec is needed.

RS-232 Port

The RS-232 port on the XStend Board shares FPGA pins with the XSA Board Flash RAM and seven-segment LED, and with the XStend Board SRAM, DIP switch, bargraph LED and IDE interface.

The Flash RAM, SRAM, and IDE interface can be deselected using their respective chip-select or read/write signals, so these components can be used simultaneously in an application with the RS-232 port. The RS-232 port has resistors on its outputs that drive the FPGA pins so these signals will be overridden by the Flash RAM, SRAM or IDE signals when they are active.

The DIP switch and LEDs (on both the XSA and XStend Boards) do not have chip-selects. Therefore, these components cannot be used in applications where the RS-232 port is needed.

USB Interface

The USB interface on the XStend Board shares FPGA pins with the XSA Board Flash RAM and the XStend Board SRAM and one seven-segment LED (LED2).

The Flash RAM and SRAM can be deselected using their respective chip-select signals, so these components can be used simultaneously in an application with the USB interface. The USB interface signals have resistors on the outputs that drive the FPGA pins so these signals will be overridden by the Flash RAM or SRAM signals when they are active.

The LED does not have a chip-select. Therefore, it cannot be used in applications where the USB interface port is needed.

XStend DIP Switch

The DIP switch on the XStend Board shares FPGA pins with the XSA Board Flash RAM, CPLD parallel port interface, and the /WRITE pin that controls configuration of the FPGA, and with the XStend Board SRAM, stereo audio codec and IDE interface. Therefore, the XStend Board DIP switches should be left in the OFF (OPEN) position if these other components are being used.

If the XStend Board DIP switch is used, then the Flash RAM and SRAM should not be enabled, and registers in the IDE interface should not be read or written. Position 1 of the DIP switch should be in the OFF (OPEN) position so the /WRITE signal of the FPGA can be controlled when the FPGA is being configured. There are resistors in the outputs of the codec that drive the FPGA so these signals can be overridden if the DIP switch is used. The parallel port interface programmed into the CPLD on the XSA Board must also be changed so it does not try to drive the pins of the FPGA that are already being pulled low by the DIP switch.

XStend LEDs

The seven-segment LED1 on the XStend Board shares FPGA pins with the XSA Board Flash RAM, CPLD parallel port interface and DIP switch, and with the XStend Board SRAM, stereo audio codec and IDE interface. Therefore, these components cannot be used in applications where the seven-segment LED1 on the XStend Board is needed. The parallel port interface programmed into the CPLD on the XSA Board must also be changed so it does not drive the segments of LED1 when the FPGA tries to do so.

The seven-segment LED2 on the XStend Board shares FPGA pins with the XSA Board Flash RAM, CPLD parallel port interface and DIP switch, and with the XStend Board SRAM, USB interface and IDE interface. Therefore, these components cannot be used in applications where the seven-segment LED2 on the XStend Board is needed. The parallel port interface programmed into the CPLD on the XSA Board must also be changed so it does not drive the segments of LED2 when the FPGA tries to do so.

The bargraph LED on the XStend Board shares FPGA pins with the XSA Board Flash RAM and seven-segment LED, and with the XStend Board SRAM, stereo audio codec, , RS-232 port, and IDE interface. Therefore, these components cannot be used in applications where the bargraph LED on the XStend Board is needed.

XStend IDE Interface

The IDE interface on the XStend Board shares FPGA pins with the XSA Board Flash RAM, seven-segment LED, CPLD parallel port interface and DIP switch, and with the XStend Board SRAM, RS-232 port, bargraph and seven-segment LEDs, and DIP switch.

The Flash RAM and SRAM can be deselected using their respective chip-select signals, so these components can be used simultaneously in an application with the IDE interface. The IDE interface can also be used at the same time as these other two components by activating its read or write control signal only when the Flash RAM and SRAM are deselected.

The DIP switches and LEDs (on both the XSA and XStend Boards) do not have chip-selects. Therefore, these components cannot be used in applications where the IDE interface is needed.

The RS-232 port has resistors on its outputs that drive the FPGA pins so these signals will be overridden by the IDE signals when they are active. So the RS-232 port and IDE interface can both be used in the same application.

The parallel port interface programmed into the CPLD on the XSA Board must also be changed so it does not try to drive the pins of the FPGA that are already being driven through the IDE interface.

XStend SRAM

The SRAM on the XStend Board shares FPGA pins with the XSA Board Flash RAM, seven-segment LED, CPLD parallel port interface and DIP switch, and with the XStend

Board RS-232 port, bargraph and seven-segment LEDs, DIP switch, USB interface and IDE interface.

The Flash RAM and IDE interface can be deselected using their respective chip-select or read/write signals, so these components can be used simultaneously in an application with the SRAM.

The DIP switches and LEDs (on both the XSA and XStend Boards) do not have chip-selects. Therefore, these components cannot be used in applications where the SRAM is needed.

The RS-232 port and USB interface both have resistors on their outputs that drive the FPGA pins so these signals will be overridden by the SRAM signals when they are active. So the RS-232 port, USB interface and IDE interface can all be used in the same application.

The parallel port interface programmed into the CPLD on the XSA Board must also be changed so it does not try to drive the pins of the FPGA that are already being driven on the SRAM.

A

XStend + XSA Pin Connections

The following table lists the connections between the XStend Board components and the components of the XSA Board. The columns of the table are arranged as follows:

Column 1 lists the pin number for the Spartan-II FPGA on the XSA Board. It is left blank if there is no connection to the FPGA for this function. Pins marked with * are useable as general-purpose I/O through the prototyping header; pins marked with ** can be used as general-purpose I/O only if the CPLD interface is reprogrammed so it doesn't drive this pin; pins with no marking cannot be used as general-purpose I/O at all.

Column 2 lists the pin number for the XC9572XL CPLD on the XSA Board. It is left blank if there is no connection to the CPLD for this function.

Column 3 lists the functions of other devices on the XSA Board that are connected to the associated FPGA and/or CPLD pin.

Column 4 lists the pin of the XSA prototyping header that is connected to the associated FPGA and/or CPLD pin.

Columns 5–7 list the pins of devices on the XStend Board that will connect to the FPGA and/or CPLD when the XSA Board is inserted into an XStend Board.

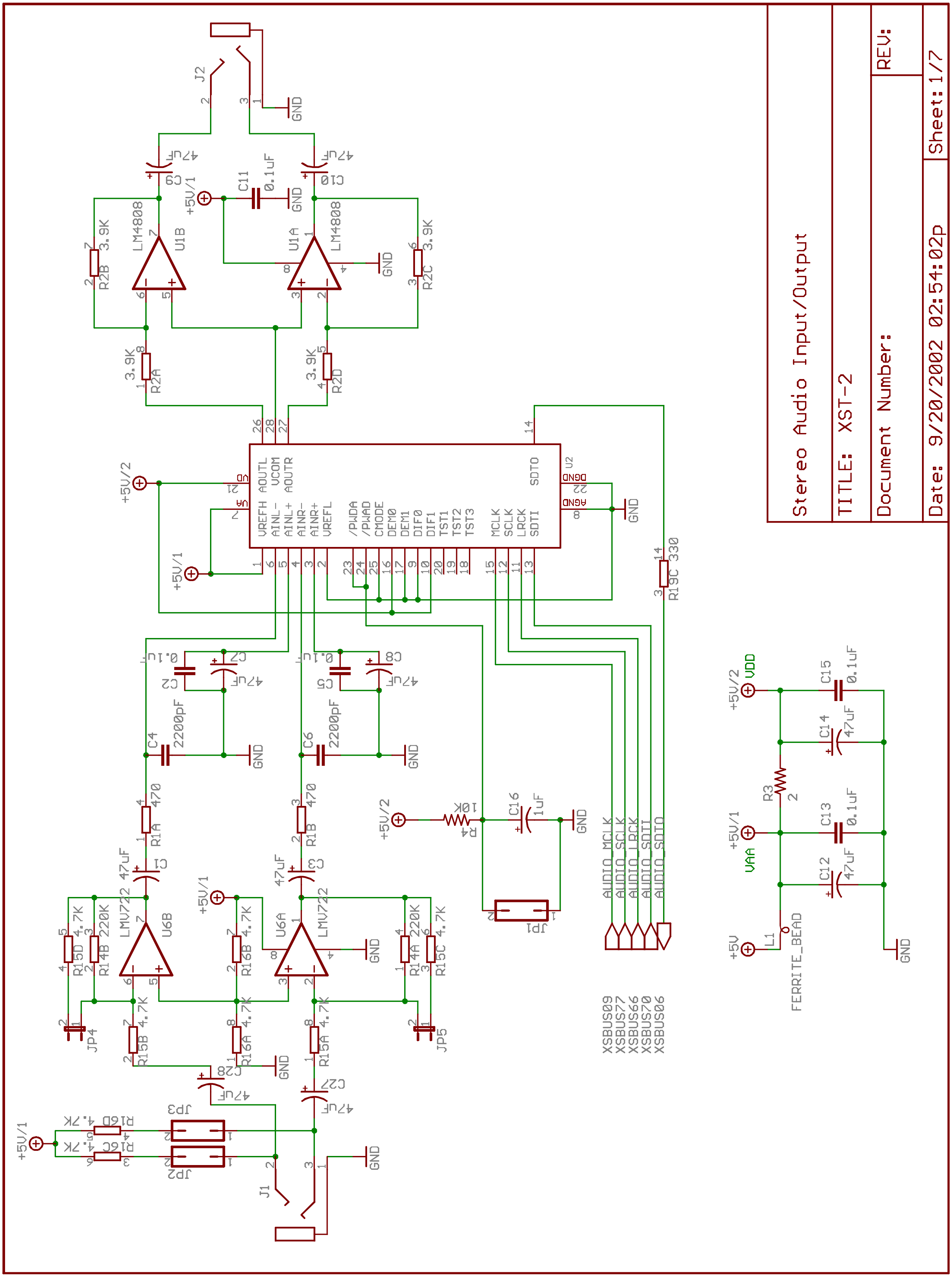
FPGA	CPLD	XSA Function	Proto. Pin	XStend V2.0 Functions		
1		+3.3V	54	+3.3V		
2	13	SPARTAN-TCK	16			
3		SDRAM-A7				
4		SDRAM-A1				
5		SDRAM-A6				
6		SDRAM-A2				
7		SDRAM-A5				
8		GND	52	GND		
9		+2.5V	22			
10		SDRAM-A3				
11		SDRAM-A4				
12*		VGA-RED0	27			
13*		VGA-RED1	28			
15*		SPARTAN-GCK3	31			
18*		SPARTAN-GCK2	1			
19*		VGA-GREEN0	29			
20*		VGA-GREEN1	32			
21*		VGA-BLUE0	33			
22*		VGA-BLUE1	34			
23*		VGA-/HSYNC	36		PUSHB4	
26*		VGA-/VSYNC	37		PUSHB3	
27*	62	FLASH-A3	50	RAM-A0	LED2-B	IDE_DMARQ
28*	63	FLASH-A2, *PARPORT-S5	51	RAM-A10	LED2-E	/USB_INT
29*	64	FLASH-A1, *PARPORT-S4	56	RAM-A11	LED2-G	USB_SUSPEND
30*	19	SPARTAN-/WRITE	69		DIPSW1	
31*	15	SPARTAN-CS	68			/IDE_RESET
32	15*	SPARTAN-TDI	15			
34	19*	SPARTAN-TDO	30			
37	16	SPARTAN-CCLK	73			
38*	18	SPARTAN-DOUT/BSY	45	RAM-A1	LED2-DP	/IDE_DMACK
39*	2	FLASH-D0,DIN/D0,LED-S1	71	RAM-A16	BARLED-9	IDE_IORDY
40*	1	FLASH-A0, *PARPORT-S3	57	RAM-A9	LED2-C	IDE_INTRQ
41*	11	FLASH-/CE	65			
42**	57	FLASH-A10, *PARPORT-D2	58	RAM-A8	LED2-F	IDE_D8
43**	12	FLASH-/OE, *PARPORT-D7	61	/RAM-OE		IDE_D9
44*	4	FLASH-D1,LED-DP	40	RAM-D6	BARLED-2	IDE_D1
46*	5	FLASH-D2,LED-S4	39	RAM-D5	BARLED-3	IDE_D2
47**	43	FLASH-A11, *PARPORT-D3	59	RAM-A13	LED2-D	IDE_D10
48**	44	FLASH-A9, *PARPORT-D1	60	RAM-A15	LED2-A	IDE_D11
49*	6	FLASH-D3,LED-S6	38	RAM-D4	BARLED-4	IDE_D3
50**	45	FLASH-A8, *PARPORT-D0	78	RAM-A14	LED1-G	IDE_D12
51**	46	FLASH-A13, *PARPORT-D5	79	RAM-A12	LED1-B	IDE_D13
54*	47	FLASH-A14,DIPSW1A	82	RAM-A7	LED1-F	/IDE_CS0
56*	48	FLASH-A17,DIPSW1D	83	RAM-A6	LED1-A	/IDE_CS1
57*	7	FLASH-D4,LED-S5	35	RAM-D3	BARLED-5	IDE_D4
58**	49	FLASH-/WE, *PARPORT-D6	62	/RAM-WE	DIPSW2	IDE_D14
59*	50	FLASH-/RESET	66	AUDIO_LRCK	BARLED-10	
60*	8	FLASH-D5,LED-S3	80	RAM-D0	BARLED-7	IDE_D6,RS232_RD
62*	9	FLASH-D6,LED-S2	81	RAM-D1	BARLED-6	IDE_D5, RS232_CTS
63*	51	FLASH-A16,DIPSW1C	84	RAM-A5	LED1-DP	IDE_DA2
64*	52	FLASH-A15,DIPSW1B	3	RAM-A4	LED1-D	IDE_DA0
65**	56	FLASH-A12, *PARPORT-D4	4	RAM-A3	LED1-C	IDE_D15
66*	58	FLASH-A7	5	RAM-A2	DIPSW5	IDE_DA1
67*	10	FLASH-D7,LED-S0	10	RAM-D2	BARLED-8	IDE_D7
68*	38	SPARTAN-/INIT	41	RAM-D7	BARLED-1	IDE_D0
69	39	SPARTAN-/PROGRAM	55		PUSHB1	
72	40	SPARTAN-DONE	53			
74*	61	FLASH-A4	70	AUDIO_SDTI	DIPSW3	
75*	60	FLASH-A5	77	AUDIO_SCLK	DIPSW4	
76*	59	FLASH-A6	6	AUDIO_SDTO	LED1-E	
77*			9	AUDIO_MCLK	DIPSW6	
78*		PARPORT-S6	67		PUSHB2	
79*			7	/RAM_CE	DIPSW8	
80*			8		DIPSW7	RS232_RTS
83*			18			RS232_TD
84*			19			USB_SCL
85*			20			USB_SDA
86*			23			/IDE_DIOR

FPGA	CPLD	XSA Function	Proto. Pin	XStend V2.0 Functions		
87*			24			/IDE_DIOW
88	42	MASTER_CLK	13	MASTER_CLK		
91		SDRAM-CLK				
93*		PS2-DATA,PUSHBUTTON	25			
94*		PS2-CLK	26			
95		SDRAM-Q0				
96		SDRAM-Q15				
99		SDRAM-Q1				
100		SDRAM-Q14				
101		SDRAM-Q2				
102		SDRAM-Q13				
103		SDRAM-Q3				
106		SPARTAN-M2	12			
109	36	SPARTAN-M0	14			
111		SPARTAN-M1	21			
112		SDRAM-Q12				
113		SDRAM-Q4				
114		SDRAM-Q11				
115		SDRAM-Q5				
116		SDRAM-Q10				
117		SDRAM-Q6				
118		SDRAM-Q9				
120		SDRAM-Q7				
121		SDRAM-Q8				
122		SDRAM-QML				
123		SDRAM-/WE				
124		SDRAM-QMH				
126		SDRAM-/CAS				
129		SDRAM-CLK				
130		SDRAM-/RAS				
131		SDRAM-CKE				
132		SDRAM-/CS				
133		SDRAM-A12				
134		SDRAM-BA0				
136		SDRAM-A11				
137		SDRAM-BA1				
138		SDRAM-A9				
139		SDRAM-A10				
140		SDRAM-A8				
141		SDRAM-A0				
142	18*	SPARTAN-TMS	17			
	30	PARPORT-C1,CPLD-TCK				
	29	PARPORT-C2,CPLD-TMS				
	28	PARPORT-C3,CPLD-TDI				
	33	PARPORT-D0				
	32	PARPORT-D1				
	31	PARPORT-D2				
	27	PARPORT-D3				
	25	PARPORT-D4				
	24	PARPORT-D5				
	23	PARPORT-D6				
	22	PARPORT-D7				
	34	PARPORT-S3				
	20	PARPORT-S4				
	35	PARPORT-S5				
	53	PARPORT-S7,CPLD-TDO				
	17	PROG-OSC				
			64	Osc-In		USB_CLKOUT

B

XSA Schematics

The following pages show the detailed schematics for the XSA Board.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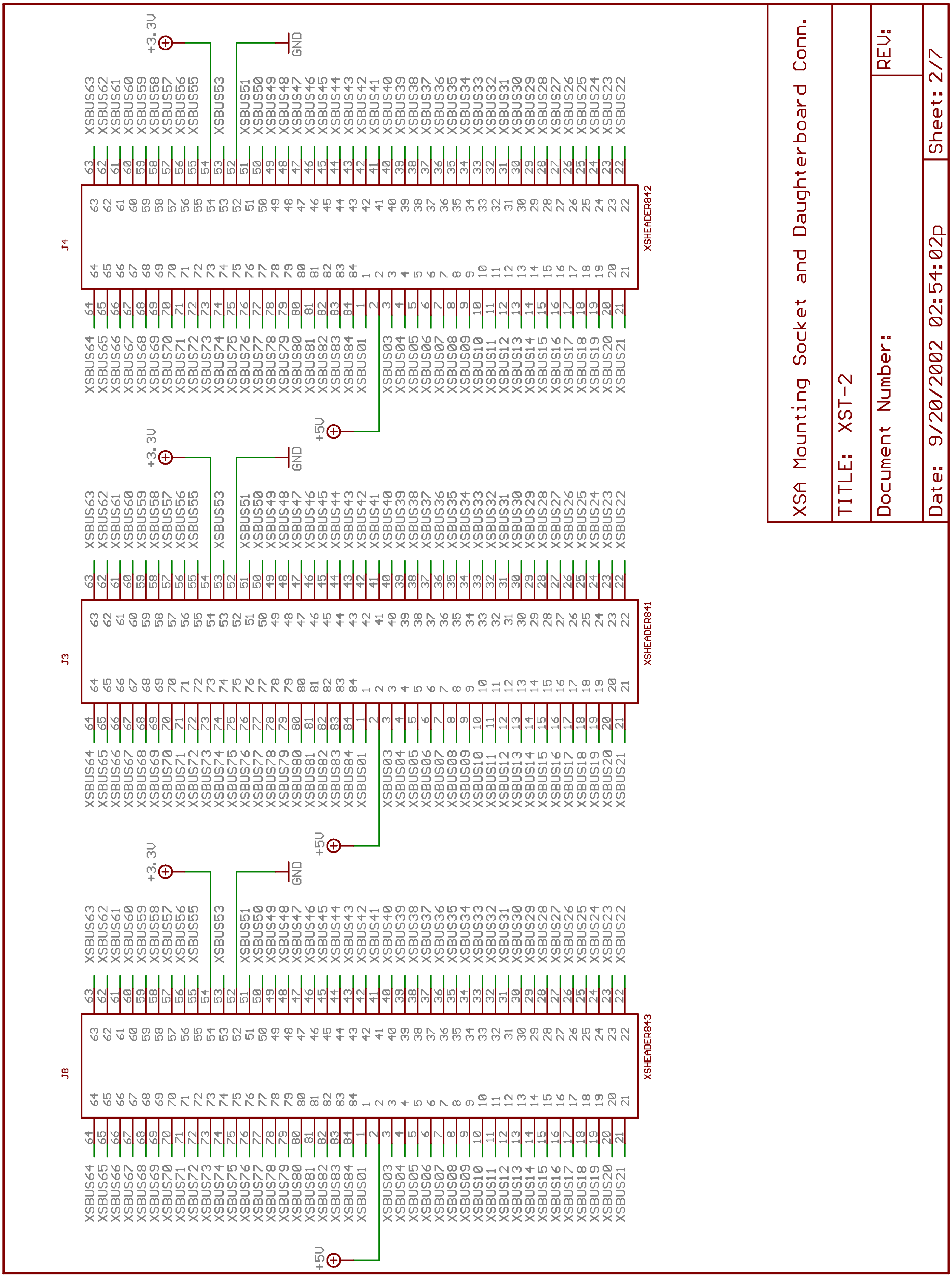
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J3
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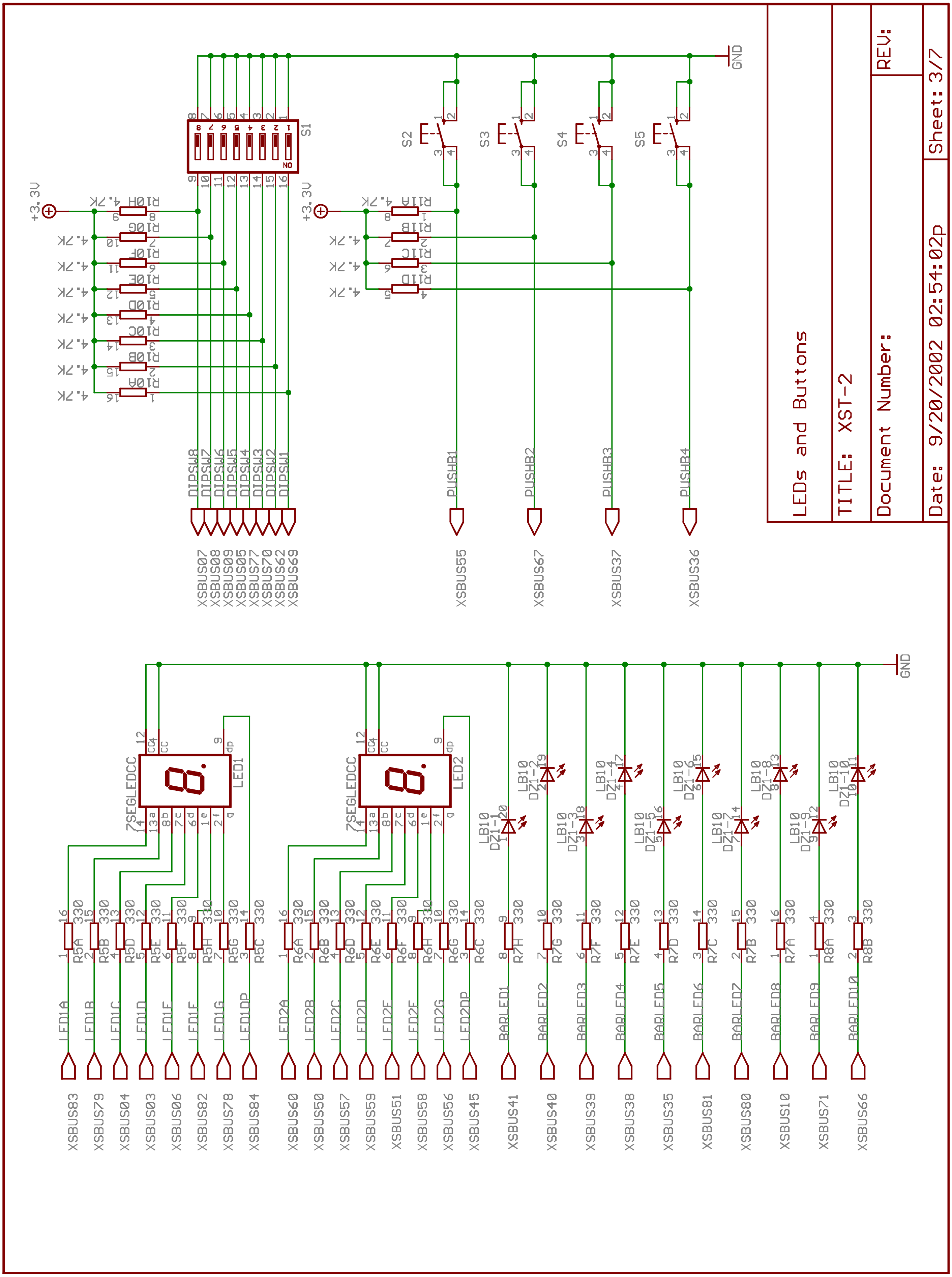
J8
XSHEADER843
+3.3V
GND
+5V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S2
S3
S4
S5
LED1
LED2
7SEGLEDCC
DIPSW1
DIPSW2
DIPSW3
DIPSW4
DIPSW5
DIPSW6
DIPSW7
DIPSW8
PUSHB1
PUSHB2
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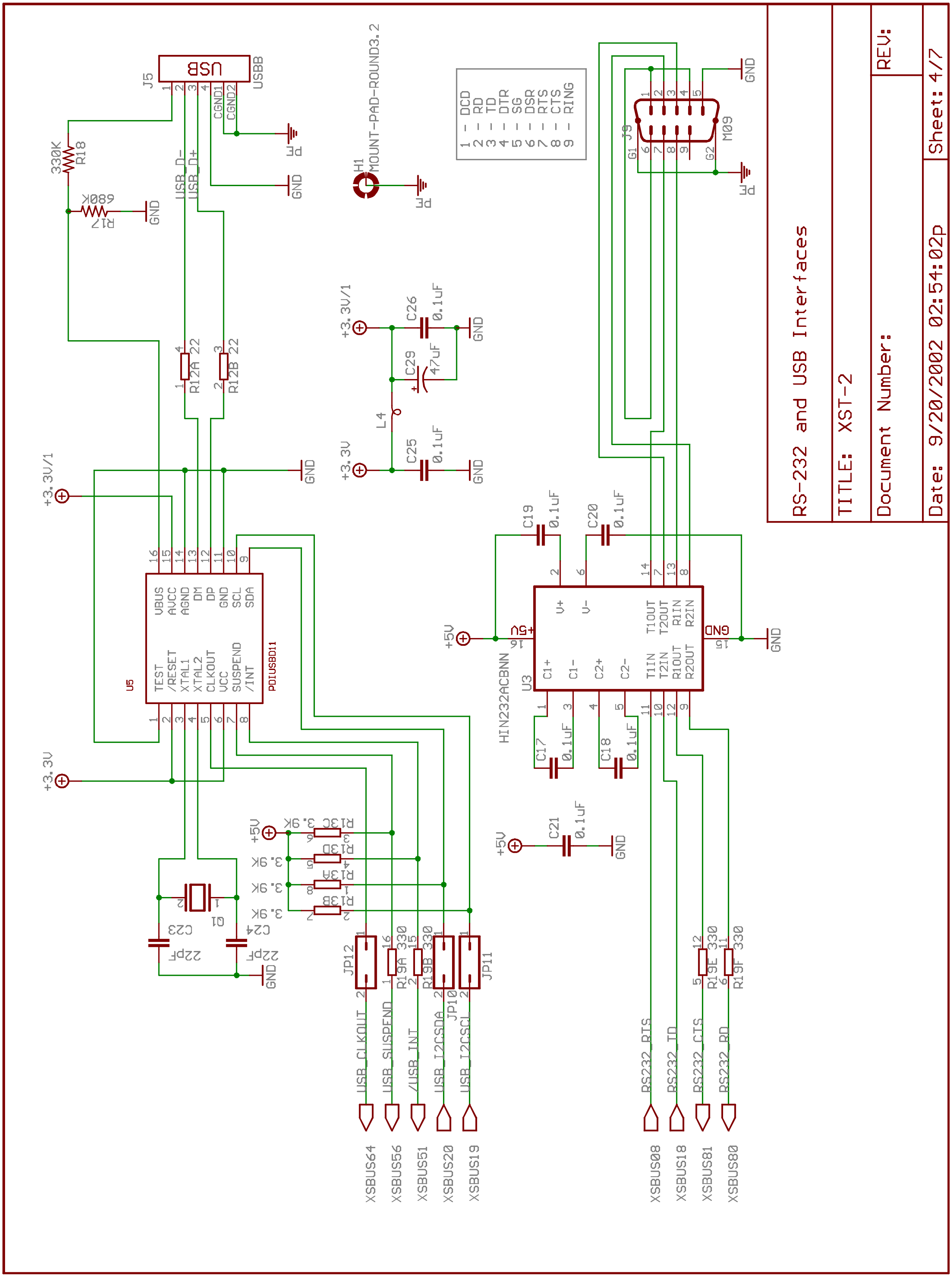
BARLED8
BARLED9
BARLED10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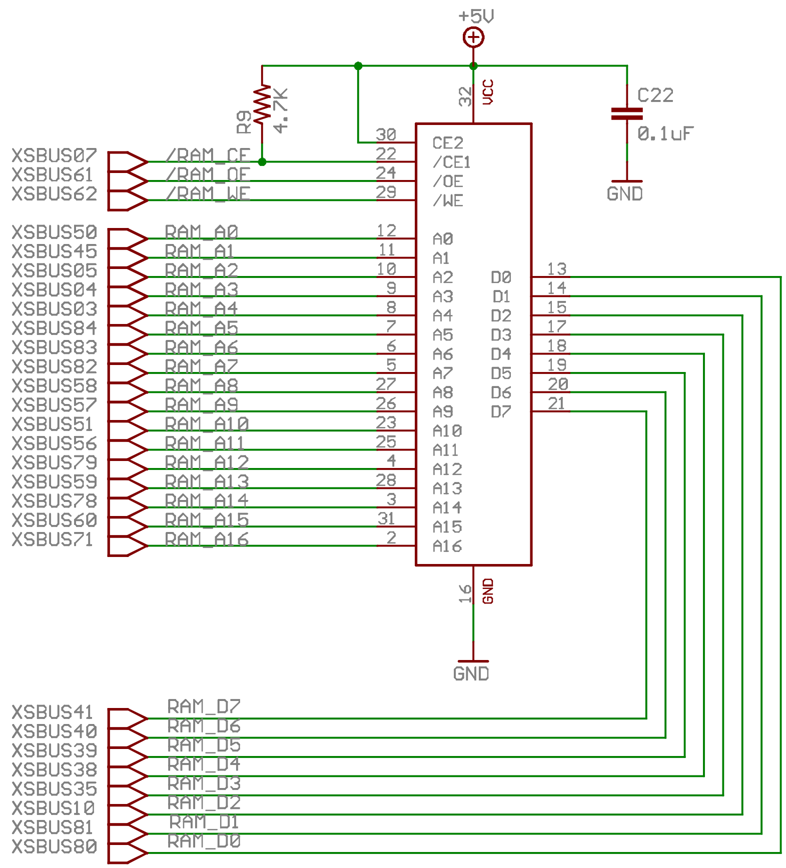

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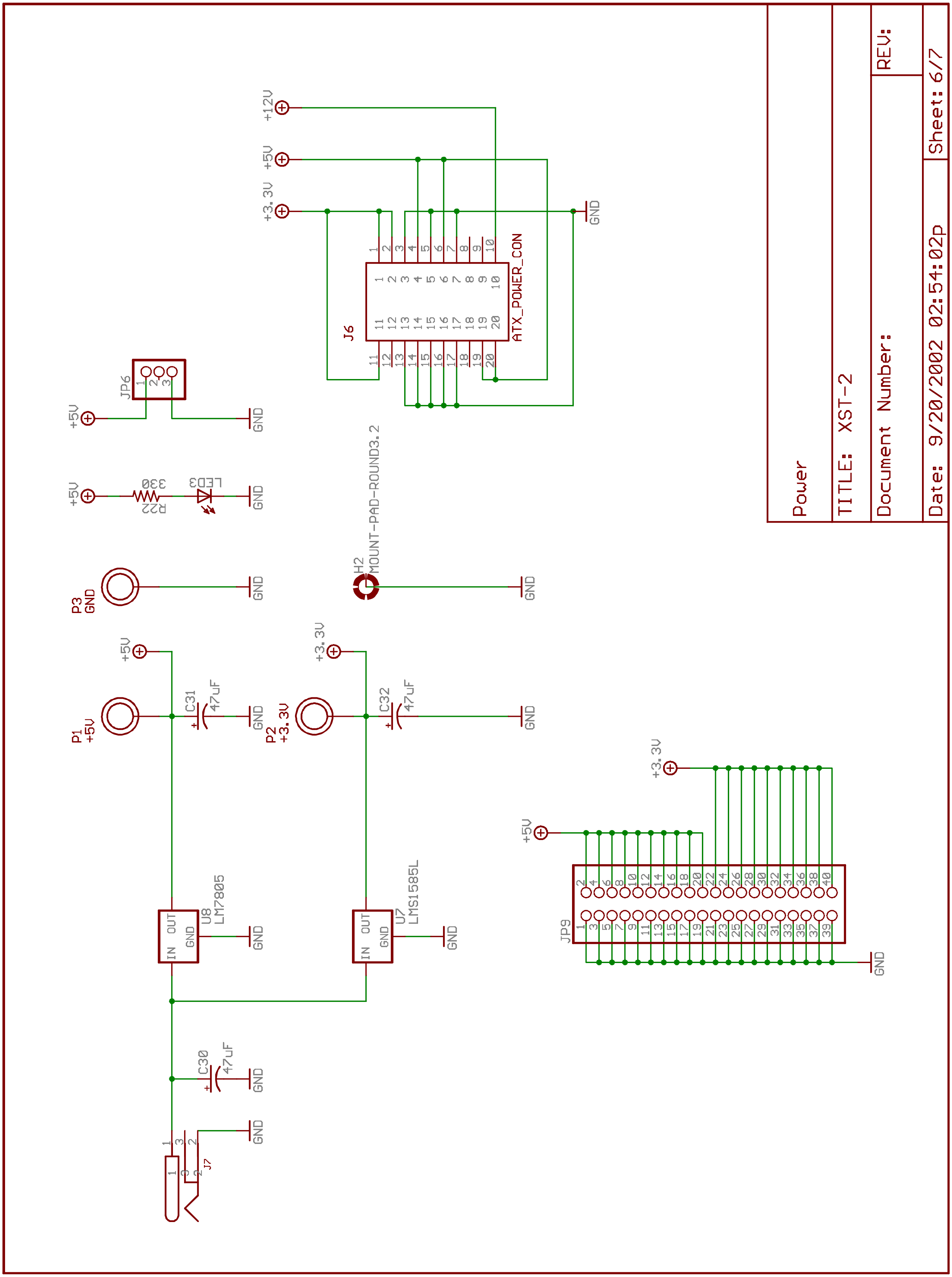
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+5V
+3.3V
GND
J6
ATX_POWER_CON
JP6
R22
330
LED3
P3
GND
H2
MOUNT-PAD-ROUND3.2
P1
+5V
C31
47uF
P2
+3.3V
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J7
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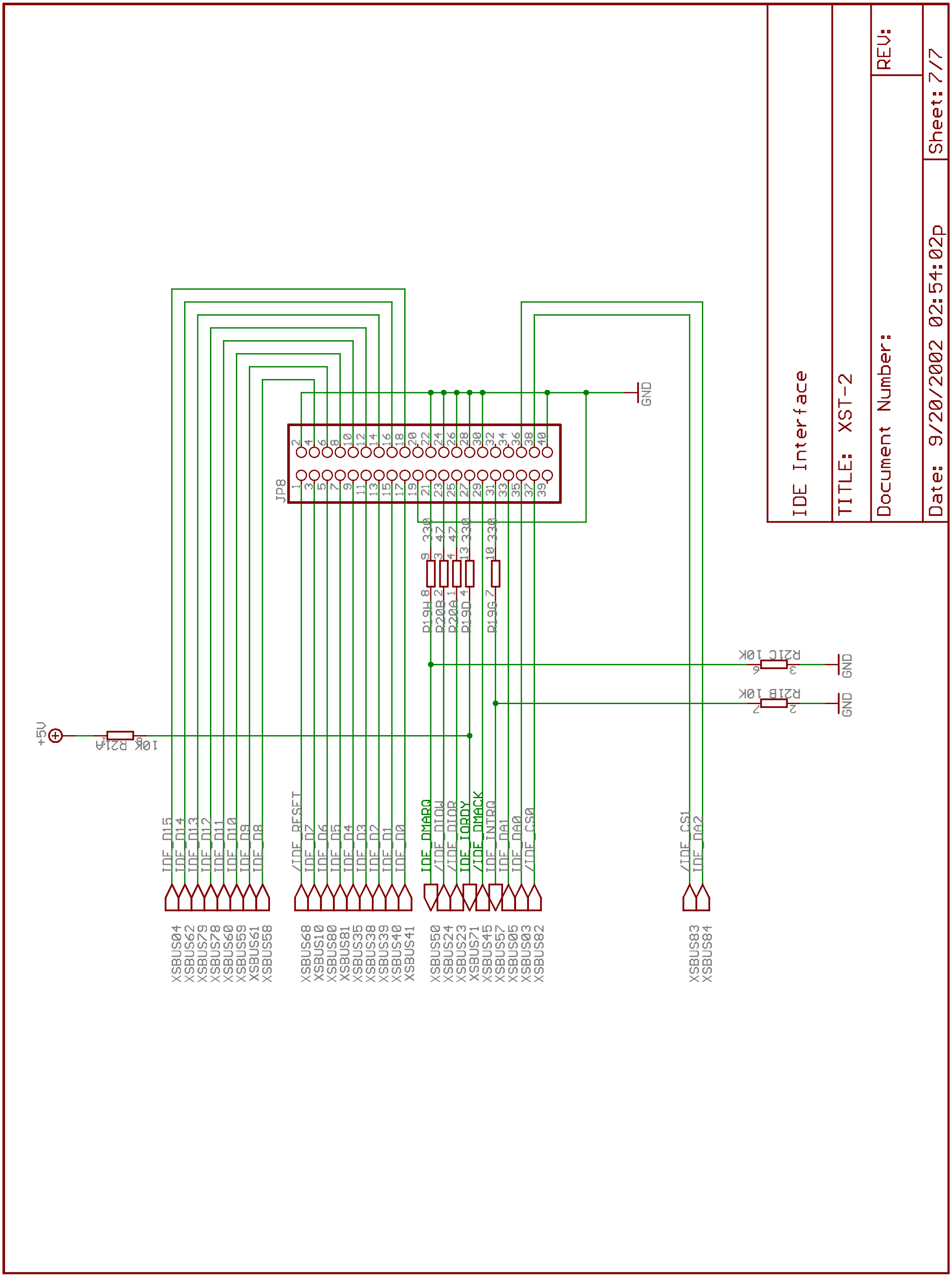
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JP8
GND
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10K R21A
R21C 10K
R21B 10K
R19H
R20B
R20A
R19D
R19G
IDE_D15
IDE_D14
IDE_D13
IDE_D12
IDE_D11
IDE_D10
IDE_D9
IDE_D8
/IDE_RESET
IDE_D7
IDE_D6
IDE_D5
IDE_D4
IDE_D3
IDE_D2
IDE_D1
IDE_D0
IDE_DMARQ
/IDE_DIOW
/IDE_DIOR
IDE_IORDY
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