XESS Corporation

# XSA-3S1000 Board V1.1 User Manual

How to install, test, and use
your new XSA-3S1000 Board

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# Table of Contents

# 1 Preliminaries

## Getting Help!

Here are some places to get help if you encounter problems:

- If you can't get the XSA-3S1000 Board hardware to work, send an e-mail message describing your problem to help@xess.com or submit a problem report at http://www.xess.com/help.html. Our web site also has
  - answers to frequently-asked-questions,
  - example designs, application notes and tutorials for the XS Boards,
  - a place to sign-up for our email forum where you can post questions to other XS Board users.
- If you can't get your XILINX WebPACK software tools installed properly, send an e-mail message describing your problem to hotline@XILINX.com or check their web site at http://www.xilinx.com/support/support.htm.
- If you need help using the WebPACK software to create designs for your XSA-3S1000 Board, then check out this tutorial.

## Take notice!!

- The XSA-3S1000 is not 5V-tolerant. Do not connect 5V logic signals to the prototyping header. Do not insert your XSA-3S1000 Board into an XST-1 or XST-2.x XStend Board. These versions of the XStend Boards contain some 5V logic.
- The XSA-3S1000 Board requires an external power supply to operate! It does not draw power through the downloading cable from the PC parallel port.
- If you are connecting a 5V - 9V DC power supply to your XSA-3S1000 Board, please make sure the center terminal of the plug is positive and the outer sleeve is negative.
- Do not power your XSA-3S1000 Board with a battery! This will not provide enough current to insure reliable operation of the XSA-3S1000 Board.
- Even if you have experience with the XILINX software tools, please read this section on setting the bitstream generation options for the XSA-3S1000 Board.

## Packing List

Here is what you should have received in your package:

- an XSA-3S1000 Board;
- a 6' cable with a 25-pin male connector on each end;
- an XSTOOLS CDROM with software utilities and documentation for using the XSA-3S1000 Board.

# 2 Installation

## Installing the XSTOOLS Utilities and Documentation

XILINX currently provides the WebPACK tools for programming their CPLDs and Spartan-series FPGAs. The XESS CDROM contains a version of WebPACK that will generate bitstream configuration files compatible with your XSA-3S1000 Board. You can also download the most current version of the WebPACK tools from the XILINX website.

In addition, XESS Corp. provides the XSTOOLS utilities for interfacing a PC to your XSA-3S1000 Board. These utilities should be installed automatically when you insert the XSTOOLS CDROM into your CDROM drive. If not, then manually run the SETUP.EXE installation program on the CDROM.

## Applying Power to Your XSA-3S1000 Board

You can use your XSA-3S1000 Board in three ways, distinguished by the method you use to apply power to the board. **Only use one of these methods to power your XSA-3S1000 Board!** Supplying power from multiple sources can damage the board and/or power supplies.

### Using a 5V - 9V DC wall-mount power supply

You can use your XSA-3S1000 Board all by itself to experiment with logic designs. Just place the XSA-3S1000 Board on a non-conducting surface as shown in Figure 1. Then apply power to the XSA-3S1000 Board from a DC wall-mount power supply with a 2.1 mm female, center-positive plug and a voltage in the range 5V – 9V. (See Figure 2 for the location of the 5V – 9V DC power jack on your XSA-3S1000 Board.) The shunt on jumper J7 should be in the "9V" position. The on-board voltage regulation circuitry will create the voltages required by the rest of the XSA-3S1000 Board circuitry. **Be careful!! The voltage regulator on the XSA-3S1000 Board can become hot.** To reduce the power dissipation in the regulator and keep it cool, use a power supply with a voltage near 5V. You can also attach a heat sink to the regulator if necessary.

### Powering Through the PS/2 Connector

You can use your XSA-3S1000 Board with a laptop PC by connecting a PS/2 male-to-male cable between the PS/2 ports of the laptop and the board. The shunt on jumper J7 should be in the "PS/2" position. The on-board voltage regulation circuitry will create the voltages required by the rest of the XSA-3S1000 Board circuitry. **Many PS/2 ports cannot supply more than 0.5A so large, high-frequency FPGA designs may not work when using this power source!**

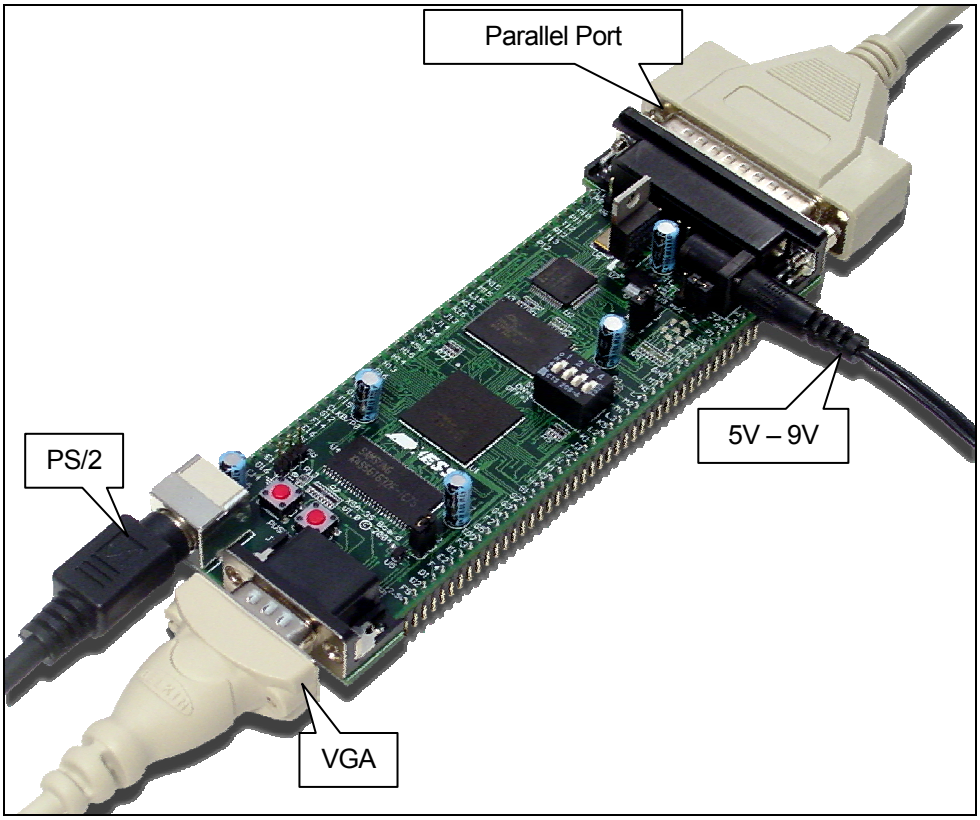
## Solderless Protoboard Installation

The two rows of pins from your XSA-3S1000 Board can be plugged into a solderless protoboard with holes spaced at 0.1" intervals. (One of the A.C.E. protoboards from 3M is a good choice.) Once plugged in, many of the pins of the FPGA are accessible to other circuits on the protoboard. (The labels printed next to the rows of pins on your XSA-3S1000 Board correspond to the pin numbers of the FPGA.) Power can still be supplied to your XSA-3S1000 Board though the 5V – 9V DC jack or the PS/2 connector as described previously.

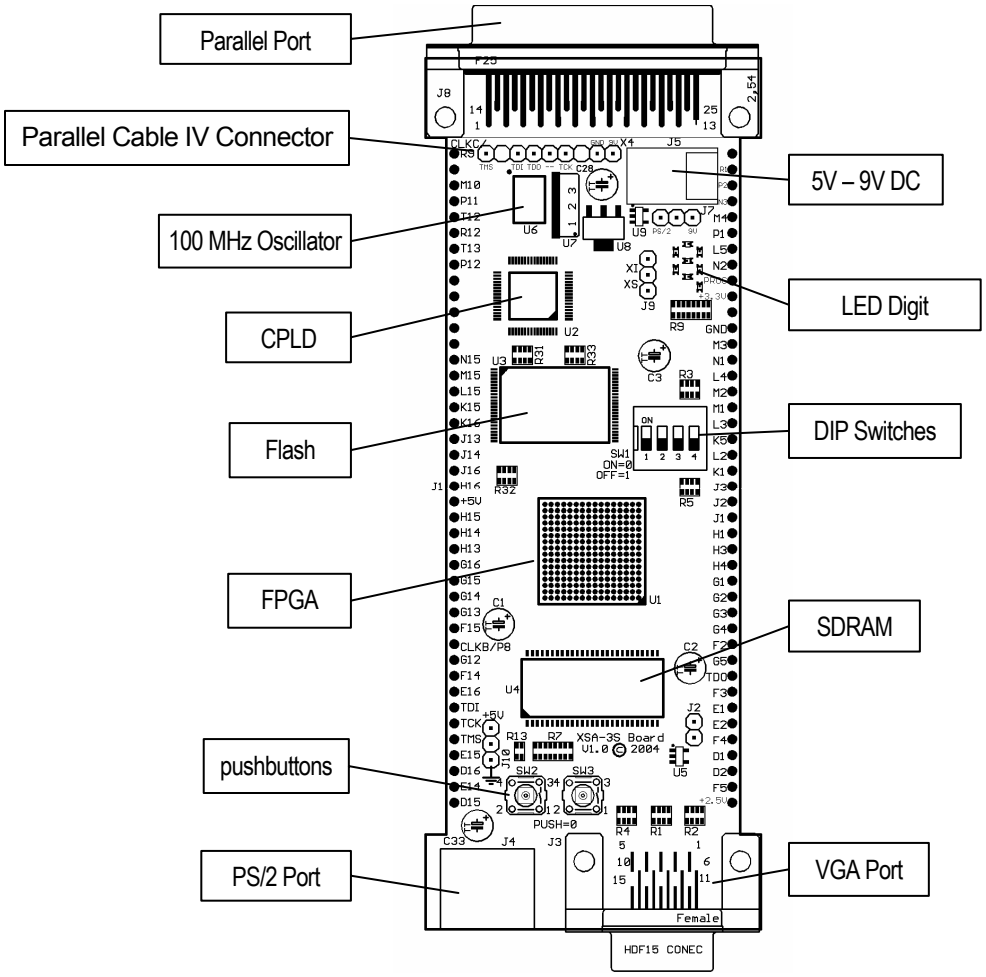
Alternatively, +5V, +3.3V, +2.5V and ground can be applied directly through several pins on the underside of the board as listed in Table 1. Remove the shunts on jumpers J2 and J7 and do not apply power through the DC jack or the PS/2 connector if you use this alternative.

• Table 1: Power supply pins for the XSA-3S1000 Board.

| Voltage | Pin | Note |
|---|---|---|
| +5V | 2 | This pin is labeled "+5V". |
| +3.3V | 54 | This pin is labeled "+3.3V". |
| +2.5V | 22 | This pin is labeled "+2.5V". |
| Ground | 52 | This pin is labeled "GND". |




• Figure 1: External connections to the XSA-3S1000 Board.




• Figure 2: Arrangement of components on the XSA-3S1000 Board.

## Connecting a PC to Your XSA-3S1000 Board

The 6' DB25 male-to-male cable included with your XSA-3S1000 Board connects it to a PC. One end of the cable attaches to the parallel port on the PC and the other connects to the female DB-25 connector at the top of the XSA-3S1000 Board as shown in Figure 1.

## Connecting a VGA Monitor to Your XSA-3S1000 Board

You can display images with up to 512 colors on a VGA monitor by connecting it to the VGA port at the bottom of your XSA-3S1000 Board (see Figure 1). You will have to create a VGA display circuit for your XSA-3S1000 Board to actually display an image. See this section for details on the VGA port circuitry and an example of a VGA display circuit.

## Connecting a Mouse or Keyboard to Your XSA-3S1000 Board

You can accept inputs from a keyboard or mouse by connecting it to the PS/2 port at the bottom of your XSA-3S1000 Board (see Figure 1). You will have to create a keyboard or mouse interface circuit to actually receive information on keystrokes or mouse movements. See this section for details on the PS/2 port circuitry and an example of a keyboard interface.

## Inserting the XSA-3S1000 Board into an XStend Board

**Do not insert an XSA-3S1000 Board into an XST-1 or XST-2.x XStend Board.** The XSA-3S1000 Board is not compatible with the voltages on these versions of the XStend Board. An XST-3.0 XStend Board will be available in 2005.

## Setting the Jumpers on Your XSA-3S1000 Board

The default jumper settings shown in Table 2 configure your XSA-3S1000 Board for use in a logic design environment. You will need to change the jumper settings only if you are:

- downloading FPGA bitstreams to your XSA-3S1000 Board using the XILINX iMPACT software;
- changing the power sources for the XSA-3S1000 supply voltages.

• Table 2: Jumper settings for XSA-3S1000 Boards.

| Jumper | Setting | Purpose |
|---|---|---|
| J2 | On (default) | A shunt should be installed if the +2.5V supply voltage is derived from the +3.3V supply. |
| | Off | The shunt should be removed if the +2.5V supply voltage is applied from an external source through pin 22 of the XSA-3S1000 Board (labeled "+2.5V" at the lower right-hand corner of the board). |
| J7 | 1-2 (9V) | The shunt should be installed on pins 1 and 2 if the board supply voltages are derived from the an external 5V – 9V DC supply. |
| | 2-3 (PS/2) | The shunt should be installed on pins 2 and 3 if the board supply voltages are derived from the +5V supply applied through the PS/2 keyboard/mouse connector (J4). |
| J9 | 1-2 (XI) | The shunt should be installed on pins 1 and 2 (XI) if the XSA-3S1000 Board is to be downloaded using the XILINX iMPACT software. |
| | 2-3 (XS) (default) | The shunt should be installed on pins 2 and 3 (XS) if the XSA-3S1000 Board is to be downloaded using the XESS GXSLOAD software. |
| J10 | N/A | This is a header that provides access to the +5V and GND references on the board. No shunt should be placed on this header. |

## Testing Your XSA-3S1000 Board

Once your XSA-3S1000 Board is installed and the jumpers are in their default configuration, you can test the board using the GUI-based GXSTEST utility as follows.

You start GXSTEST by clicking on the 

icon placed on the desktop during the XSTOOLS installation. This brings up the window shown below.


Next you select the parallel port that your XSA-3S1000 Board is connected to from the Port pulldown list. GXSTEST starts with parallel port LPT1 as the default, but you can also select LPT2 or LPT3 depending upon the configuration of your PC.

After selecting the parallel port, pick the XSA-3S1000 item in the Board Type pulldown list. Then click on the TEST button to start the testing procedure. GXSTEST will configure the FPGA to perform a test procedure on your XSA-3S1000 Board. Within thirty seconds you will see a **O** displayed on the LED digit if the test completes successfully. Otherwise an **E** will be displayed if the test fails. A status window will also appear on your PC screen informing you of the success or failure of the test.

If your XSA-3S1000 Board fails the test, you will be shown a checklist of common causes for failure. If none of these causes applies to your situation, then try some of the solutions listed in the XSTOOLS\README.TXT file. If you cannot get your board to pass the test even after taking these steps, then contact XESS Corp for further assistance.

As a result of testing the XSA-3S1000 Board, the CPLD is programmed with the standard parallel port interface found in the XSTOOLS\XSA\3S1000\dwnldpar.svf bitstream file. This is the interface that should be loaded into the CPLD when you want to use it with the GXSLOAD utility.

## Setting the XSA-3S1000 Board Clock Oscillator Frequency

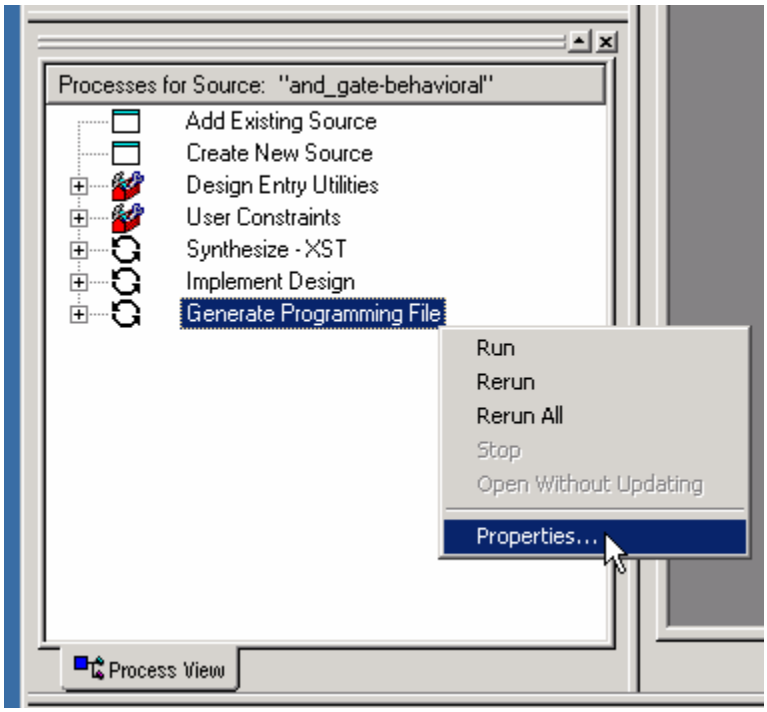
Unlike previous versions of the XSA Board, your XSA-3S1000 Board has a fixed-frequency oscillator of 100 MHz. The GXSSETCLK utility cannot be used to change the frequency of the clock sent to the FPGA and CPLD. You can lower the clock frequency by placing a clock-divider circuit in the FPGA or CPLD. See the section on the XSA-3S1000 Board clock circuitry for more details.

# 3 Programming

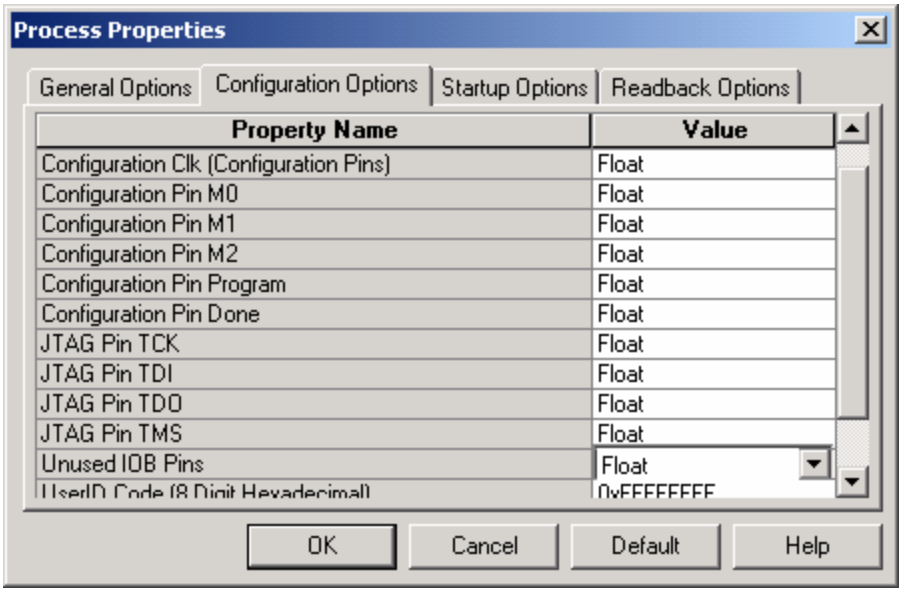
This section will show you how to download logic designs into the FPGA and CPLD of your XSA-3S1000 Board and how to download and upload data to and from the SDRAM and Flash devices on the board.

## Generating Bitstreams for the FPGA

Before downloading a bitstream to the FPGA on your XSA-3S1000 Board, you will use the XILINX development software to generate the .BIT file. Steps for doing this are given in the XILINX documentation, but there is one detail that is specific to your board. The Spartan3 FPGA has relatively low-impedance, internal pullup and pulldown resistors on its pins that become active after the FPGA is configured. These resistors can overpower the 4.7KΩ external pullup and pulldown resistors on the board and prevent it from functioning correctly. Therefore, you have to set the bitstream generation options to disable these internal resistors. This is done by right-clicking on the Generate Programming File item in the Processes pane and selecting Properties… from the pop-up menu.



Then select the Configuration Options tab in the Process Properties window and change all the pin settings to float. Then click on the OK button. The internal pullup and pulldown resistors will now be disabled in the bitstream generated for this project.



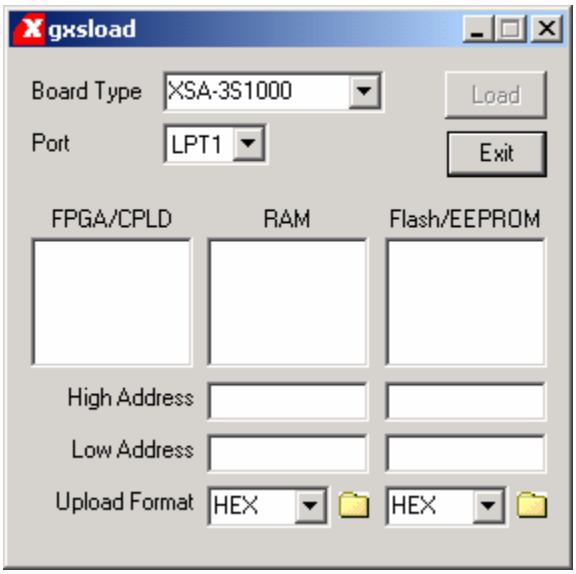

# Downloading Bitstreams into the FPGA and CPLD

## Downloading Using GXSLOAD

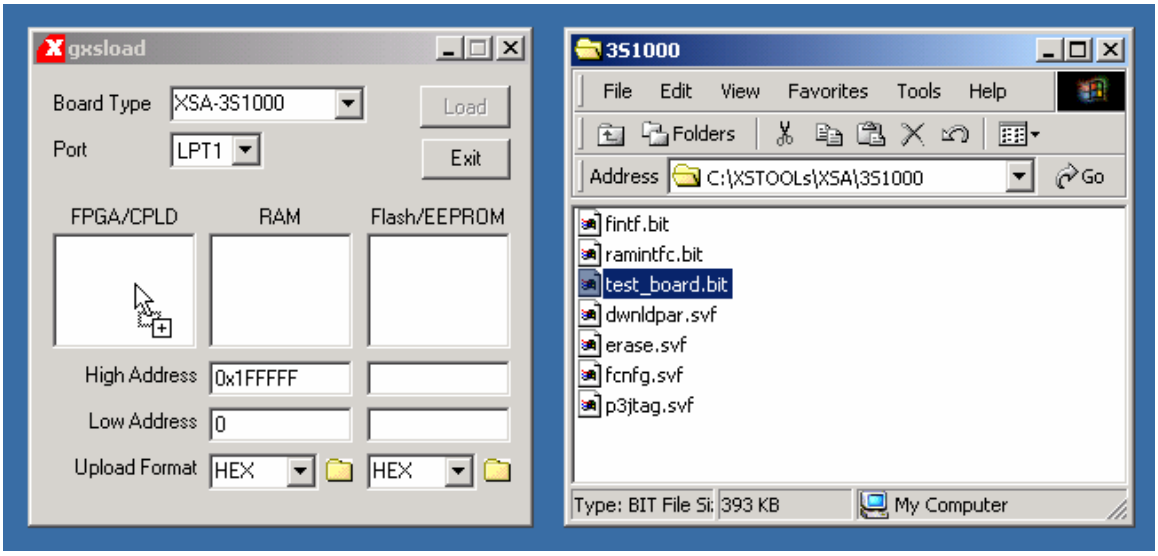
As you develop and test a logic design, you will usually connect the XSA-3S1000 Board to the parallel port of a PC and download the configuration bitstream each time you make changes. You can download a bitstream into your XSA-3S1000 Board using the GXSLOAD utility.

You start GXSLOAD by clicking on the 

icon placed on the desktop during the XSTOOLS installation. This brings up the window shown below. Select the XSA-3S1000 Board and the parallel port to which it is connected as indicated below.

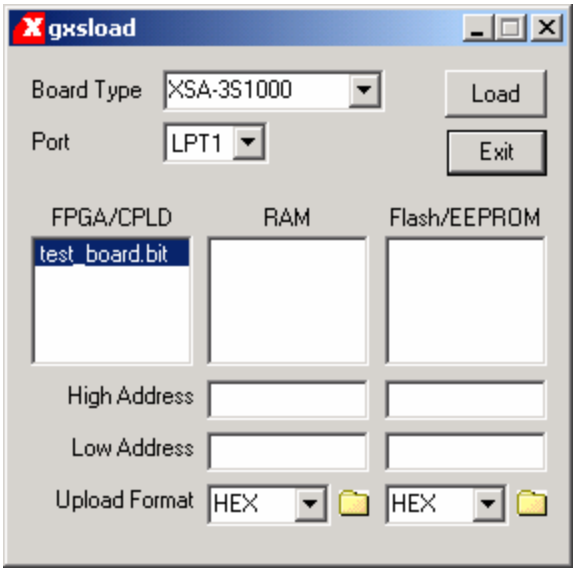



Now you can download bitstream files to the FPGA or CPLD simply by dragging them from their folder and dropping them into the FPGA/CPLD pane of the GXSLOAD window as shown below.

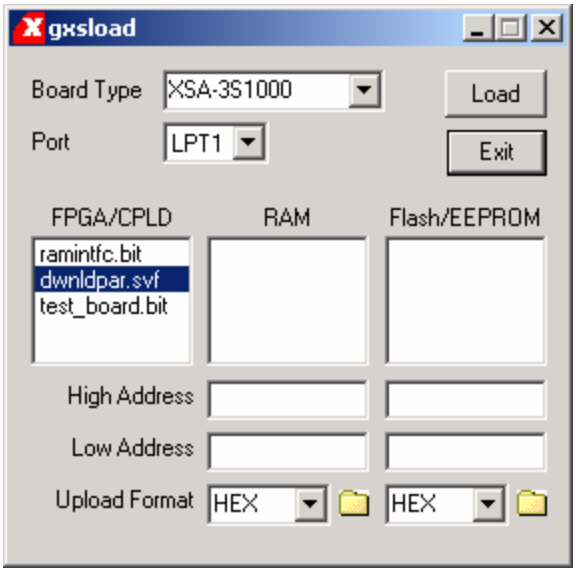



Once you drop the file, the highlighted file name appears in the FPGA/CPLD pane and the Load button in the GXSLOAD window is enabled. Clicking on the Load button will begin sending the bitstream in the file to the XSA-3S1000 Board through the parallel port connection. .BIT files contain configuration bitstreams that are loaded into the FPGA while .SVF files will go to the CPLD. GXSLOAD will reject any non-downloadable files (ones

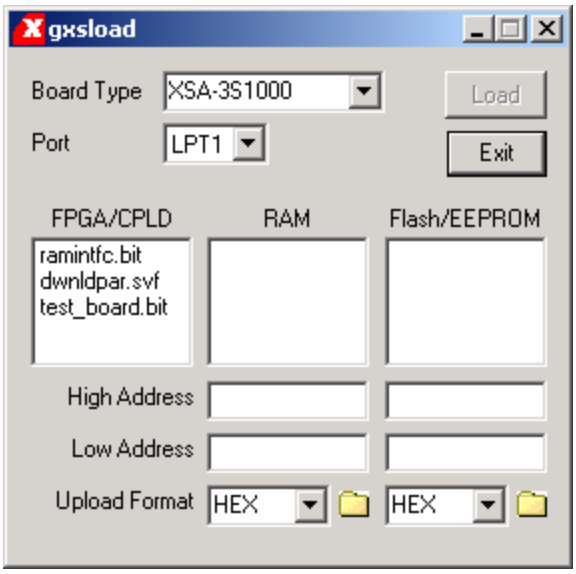
with a suffix other than .BIT or .SVF). During the downloading process, GXSLOAD will display the name of the file and the progress of the current download.




You can drag & drop multiple files into the FPGA/CPLD area. Clicking your mouse on a filename will highlight the name and select it for downloading. Only one file at a time can be selected for downloading.



Double-clicking the highlighted file will deselect it so no file will be downloaded. Doing this disables the Load button.




### Downloading Using Xilinx iMPACT

You can use the Xilinx iMPACT software to download bitstreams to the XSA-3S1000 Board. The iMPACT programming tool downloads bitstreams through the JTAG interface of the FPGA so we need to change the parallel port interface by reprogramming the CPLD. Drag & drop the p3jtag.svf file from the XSTOOLS\XSA\3S1000 folder into the FPGA/CPLD pane of the GXSLOAD window. Then click on the Load button and the CPLD will be reprogrammed in less than a minute. Then move the shunt on jumper J9 from the XS to the XI position. At this point you can start iMPACT and it will believe it is connected to the XSA-3S1000 Board through a Xilinx Parallel Cable III in boundary-scan mode. Follow the instructions for iMPACT to download bitstreams to the FPGA.

You can also use a Xilinx Parallel Cable IV with the XSA-3S1000 Board by downloading the XSTOOLS\XSA\3S1000\p4jtag.svf file into the CPLD. Then disconnect the XESS downloading cable and connect the Xilinx Parallel Cable IV to the X4 connector. Now start iMPACT to download bitstreams to the FPGA in boundary-scan mode.

Note that the CPLD only needs to be reprogrammed once to support iMPACT because it retains its configuration even when power is removed from the board. (If you want to go back to using the GXSLOAD programming utility, just must move the shunt on J9 back to the XS position and download the XSTOOLS\XSA\dwnldpar.svf file into the CPLD.)

## Storing Non-Volatile Bitstreams in the Flash

The FPGA on the XSA-3S1000 Board stores its configuration in an on-chip SRAM which is erased whenever power is removed. Once your design is finished, you may want to store the bitstream in the 16 Mbit Flash device on the XSA-3S1000 Board from which the FPGA will be configured each time power is applied.

The Flash is partitioned into four quadrants, each of which can hold a bitstream for the FPGA. Before a bitstream can be downloaded into a quadrant of the Flash, the .BIT file must be converted into an .EXO or .MCS format using one of the following commands:

| Quadrant | Address Range | Conversion Command | DIP Switch Setting | |
|---|---|---|---|---|
| | | | SW1-1 | SW1-2 |
| 0 | 0x000000 – 0x07FFFF | promgen –u 0 file.bit –p exo -w<br>promgen –u 0 file.bit –p mcs –w | ON | ON |
| 1 | 0x080000 – 0x0FFFFF | promgen –u 80000 file.bit –p exo -w<br>promgen –u 80000 file.bit –p mcs –w | ON | OFF |
| 2 | 0x100000 – 0x17FFFF | promgen –u 100000 file.bit –p exo -w<br>promgen –u 100000 file.bit –p mcs –w | OFF | ON |
| 3 | 0x180000 – 0x1FFFFF | promgen –u 180000 file.bit –p exo -w<br>promgen –u 180000 file.bit –p mcs -w | OFF | OFF |

In the commands shown above, the bitstream in file.bit is transformed into an .EXO or .MCS formatted file starting at the first address in each quadrant and proceeding upward.

The .EXO or .MCS file is downloaded into the Flash device by dragging it into the Flash/EEPROM pane and clicking on the Load button. This activates the following sequence of steps:

1. The FPGA and CPLD on the XSA-3S1000 Board are reprogrammed to create an interface between the Flash device and the PC parallel port.

2. The entire Flash device is erased.

3. The contents of the .EXO or .MCS file are downloaded into the Flash through the parallel port.

4. The CPLD is reprogrammed with a circuit that configures the FPGA with the contents of the Flash whenever power is applied to the XSA-3S1000 Board. (This configuration loader is stored in the XSTOOLS\XSA\3S1000\fcnfg.svf file.)

Once the Flash download is complete, you must set the DIP switches to select the Flash quadrant containing the FPGA bitstream (see the switch settings in the table above). The FPGA will be configured with the bitstream in that quadrant whenever power is applied to the board. You can download multiple bitstreams to the Flash and use the switches to select the one to be loaded into the FPGA on power-up.

Multiple files can be stored in the Flash device just by dragging them into the Flash/EEPROM area, highlighting the files to be downloaded and clicking the Load button. (Note that anything previously stored in the Flash will be erased by each new download.) This is useful if you need to store information in the Flash in addition to the FPGA bitstream. Files are selected and de-selected for downloading just by clicking on their names in the Flash/EEPROM area. **The address ranges of the data in each file should not overlap or this will corrupt the data stored in the Flash device!**

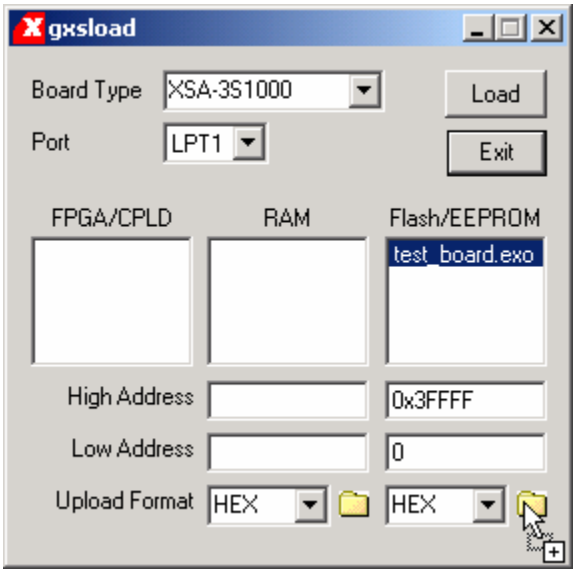
You can also examine the contents of the Flash device by uploading it to the PC. To upload data from an address range in the Flash, type the upper and lower bounds of the range into the High Address and Low Address fields located below the Flash/EEPROM pane, and select the format for the uploaded data from the Upload Format pulldown list.

Then click on the file icon and drag & drop it into any folder. This activates the following sequence of steps:

1. The CPLD and FPGA on the XSA-3S1000 Board are reprogrammed to create an interface between the Flash device and the PC parallel port.

2. The Flash data between the high and low addresses (inclusive) is uploaded through the parallel port.

3. The uploaded data is stored in a file named FLSHUPLD with an extension that reflects the file format.




The uploaded data can be stored in the following formats:

MCS: Intel hexadecimal file format. This is the same format generated by the promgen utility with the –p mcs option.

HEX: Identical to MCS format.

EXO-16: Motorola S-record format with 16-bit addresses (suitable for 64 KByte uploads only).

EXO-24: Motorola S-record format with 24-bit addresses. This is the same format generated by the promgen utility with the –p exo option.

EXO-32: Motorola S-record format with 32-bit addresses.

XESS-16: XESS hexadecimal format with 16-bit addresses. (This is a simplified file format that does not use checksums.)

XESS-24: XESS hexadecimal format with 24-bit addresses.

XESS-32: XESS hexadecimal format with 32-bit addresses.

After the data is uploaded from the Flash, the default parallel port interface remains in the CPLD. You will need to reprogram the CPLD with the configuration loader bitstream in XSTOOLS\XSA\3S1000\fcnfg.svf if you want the FPGA to be configured from Flash whenever power is applied.

## Downloading and Uploading Data to the SDRAM

The XSA-3S1000 Board contains a 256 Mbit, synchronous DRAM (16M x 16 SDRAM) whose contents can be downloaded and uploaded by GXSLOAD. This is useful for initializing the SDRAM with data for use by the FPGA and then reading the SDRAM contents after the FPGA has operated upon it. The SDRAM is loaded with data by dragging & dropping one or more .EXO, .MCS, .HEX, and/or .XES files into the RAM pane of the GXSLOAD window and then clicking on the Load button. This activates the following sequence of steps:

1. The FPGA is reprogrammed to create an interface between the SDRAM and the PC parallel port. (This interface is stored in the XSTOOLS\XSA\3S1000\ramintfc.bit bitstream file. **The CPLD must have previously been loaded with the dwnldpar.svf file found in the same folder.**)

2. The contents of the .EXO, .MCS, .HEX or .XES files are downloaded into the SDRAM through the parallel port. **The data in the files will overwrite each other if their address ranges overlap.**

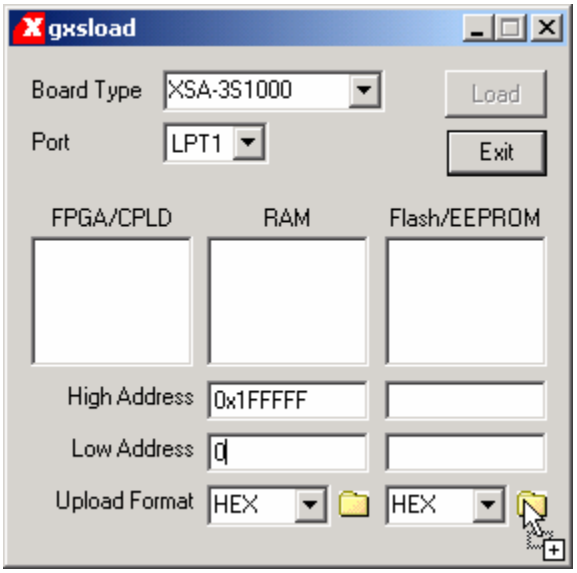
3. If any file is highlighted in the FPGA/CPLD pane, then this bitstream is loaded into the FPGA or CPLD on the XSA-3S1000 Board. Otherwise the FPGA remains configured as an interface between the PC and the SDRAM.

You can also examine the contents of the SDRAM device by uploading it to the PC. To upload data from an address range in the SDRAM, type the upper and lower bounds of the range into the High Address and Low Address fields below the RAM pane, and select the format for the uploaded data from the Upload Format pulldown list. Then click on the file icon and drag & drop it into any folder. This activates the following sequence of steps:

1. The FPGA is reprogrammed to create an interface between the SDRAM device and the PC parallel port.

2. The SDRAM data between the high and low addresses (inclusive) is uploaded through the parallel port.

3. The uploaded data is stored in a file named RAMUPLD with an extension that reflects the file format.




The 16-bit data words in the SDRAM are mapped into the eight-bit data format of the .HEX, .MCS, .EXO and .XES files using a Big Endian style. That is, the 16-bit word at location *N* in the SDRAM is stored in the eight-bit file with the upper eight bits at address *2N* and the lower eight bits at address *2N+1*. This byte-ordering applies for both RAM uploads and downloads.

# 4

# Programmer's Models

This section describes the various sections of the XSA-3S1000 Board and shows how the I/O of the FPGA and CPLD are connected to the rest of the circuitry. The schematics which follow are less detailed so as to simplify the descriptions. For more information, you can find a table of FPGA and CPLD pin connections and detailed schematics at the end of this manual.

## XSA-3S1000 Board Organization

The XSA-3S1000 Board contains the following components:

FPGA: This is the main repository of programmable logic on the XSA-3S1000 Board.

CPLD: This manages the interface between the PC parallel port and the rest of the XSA-3S1000 Board. It can also configure the FPGA with a bitstream from Flash.

Oscillator: A fixed-frequency oscillator generates the master clock for the XSA-3S1000 Board.

SDRAM: A 256 Mbit SDRAM provides volatile data storage accessible by the FPGA.

Flash: A 16 Mbit Flash device provides non-volatile storage for data and FPGA configuration bitstreams.

LED: A seven-segment LED allows visible feedback as the XSA-3S1000 Board operates.

DIP switch: A four-position DIP switch passes settings to the XSA-3S1000 Board and controls the upper address bits of the Flash device.

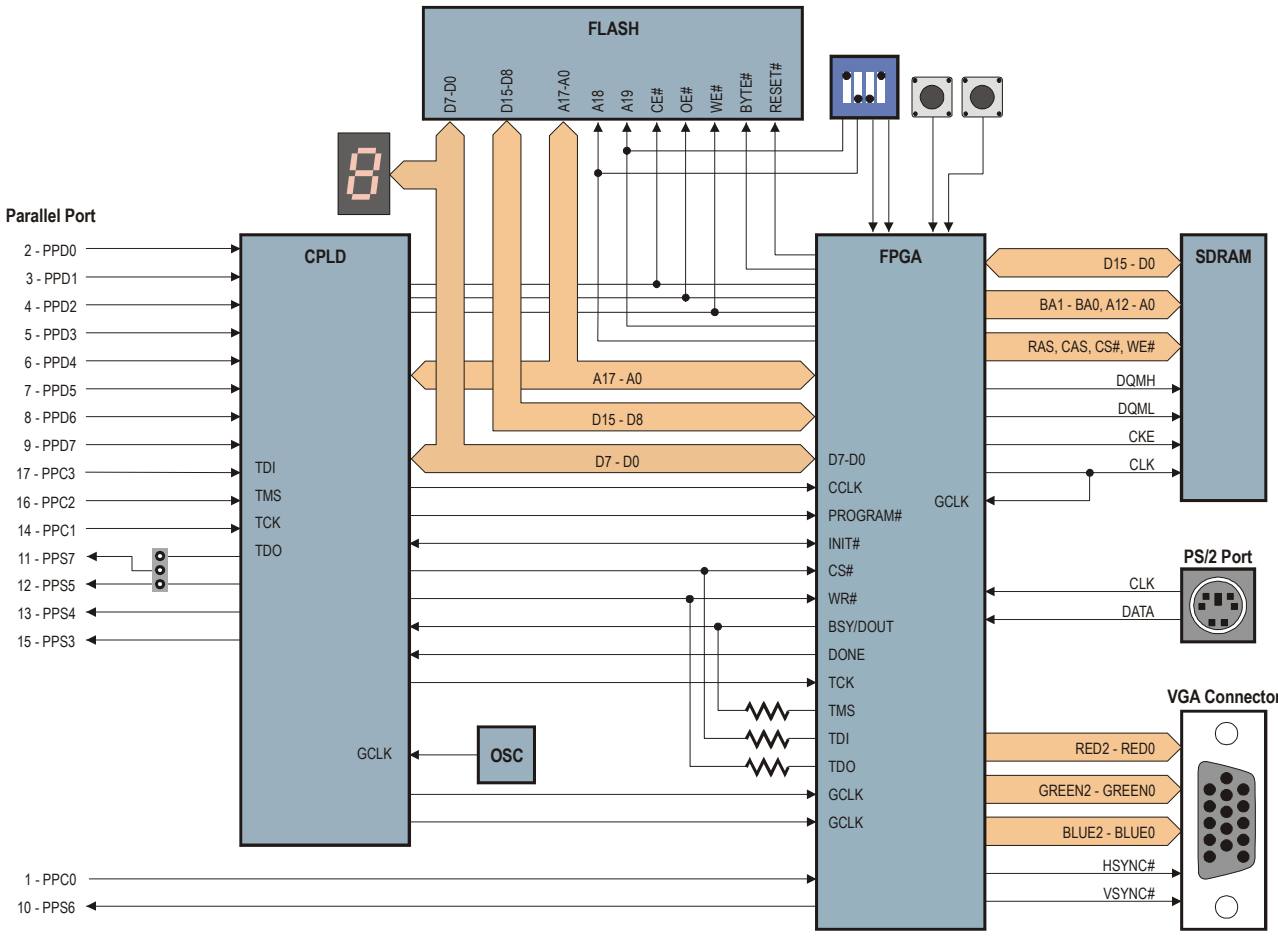
Pushbuttons: Two pushbuttons send momentary contact information to the FPGA.

PS/2 Port: A keyboard or mouse can interface to the XSA-3S1000 Board through this port.

VGA Port: The XSA-3S1000 Board can send signals to display 512-color graphics on a VGA monitor through this port.

Parallel Port: This is the main interface for passing configuration bitstreams and data to and from the XSA-3S1000 Board.

Prototyping Header: Many of the FPGA I/O pins are connected to the 84 pins on the bottom of the XSA-3S1000 Board that are meant to mate with solderless breadboards or an XST-3 Board.




• Figure 3: XSA-3S1000 Board programmer's model.

## Programmable logic: FPGA and CPLD

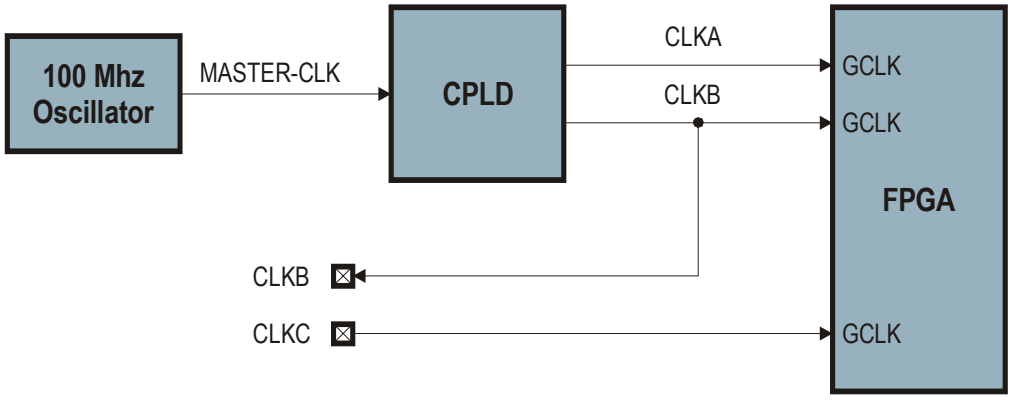
The XSA-3S1000 Board contains two programmable logic chips:

- A 1,000,000-gate XILINX Spartan3 FPGA in a 256-pin BGA package (XC3S1000-4FT256) is the main repository of programmable logic on the XSA-3S1000 Board.
- A XILINX XC9500XL CPLD (XC9572XL-10VQ64) is used to manage the configuration of the FPGA via the parallel port. In stand-alone mode, the CPLD also configures the FPGA with a bitstream from the Flash RAM.

## 100 MHz Fixed-Frequency Oscillator

An oscillator provides a fixed, 100 MHz clock signal to a dedicated clock input of the CPLD. From this clock, the CPLD generates two clock signals, CLKA and CLKB, that go to dedicated clock inputs of the FPGA. This allows the CPLD to control the FPGA clocks. By default, the CPLD outputs 100 MHz and 50 MHz clocks on CLKA and CLKB, respectively. The clock-divider circuit in the CPLD can be reprogrammed to send lower-frequency clocks to the FPGA if desired.

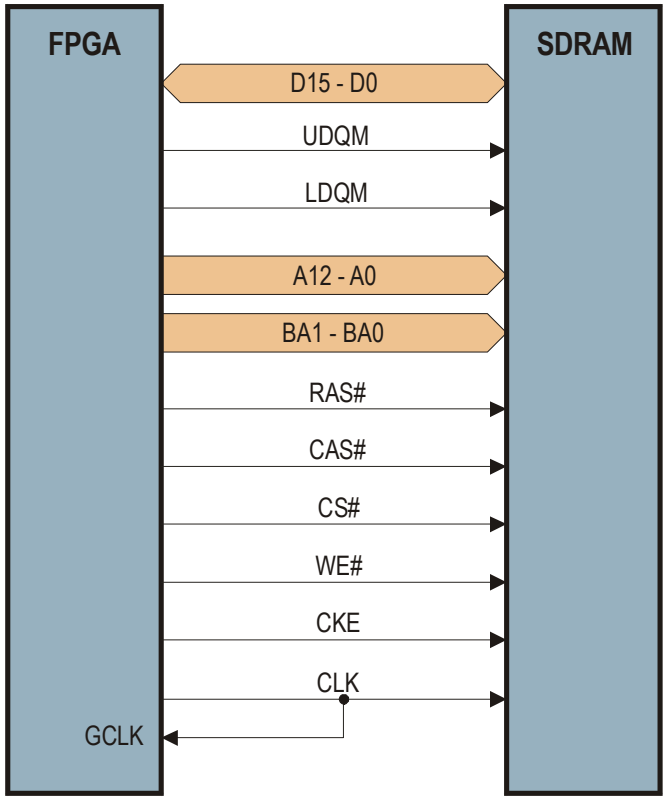
The CLKB signal also exits through a pin on the prototyping header, so it can be used as a clock for an external system connected to the XSA-3S1000 Board. Or the external system can send a clock directly to the FPGA through the dedicated CLKC pin of the prototyping header.



## Synchronous DRAM

The XSA-3S1000 Board incorporates a 16M x 16 SDRAM (K4S561632ETC75) that connects solely to the FPGA as shown below. Note that the clock signal is re-routed back to a dedicated clock input of the FPGA to compensate for clock delays to the SDRAM, thus allowing synchronization of the FPGA's internal operations with the SDRAM operations.

This application note describes an SDRAM controller that makes the SDRAM appear like a simple static RAM to the rest of the circuitry in the FPGA.



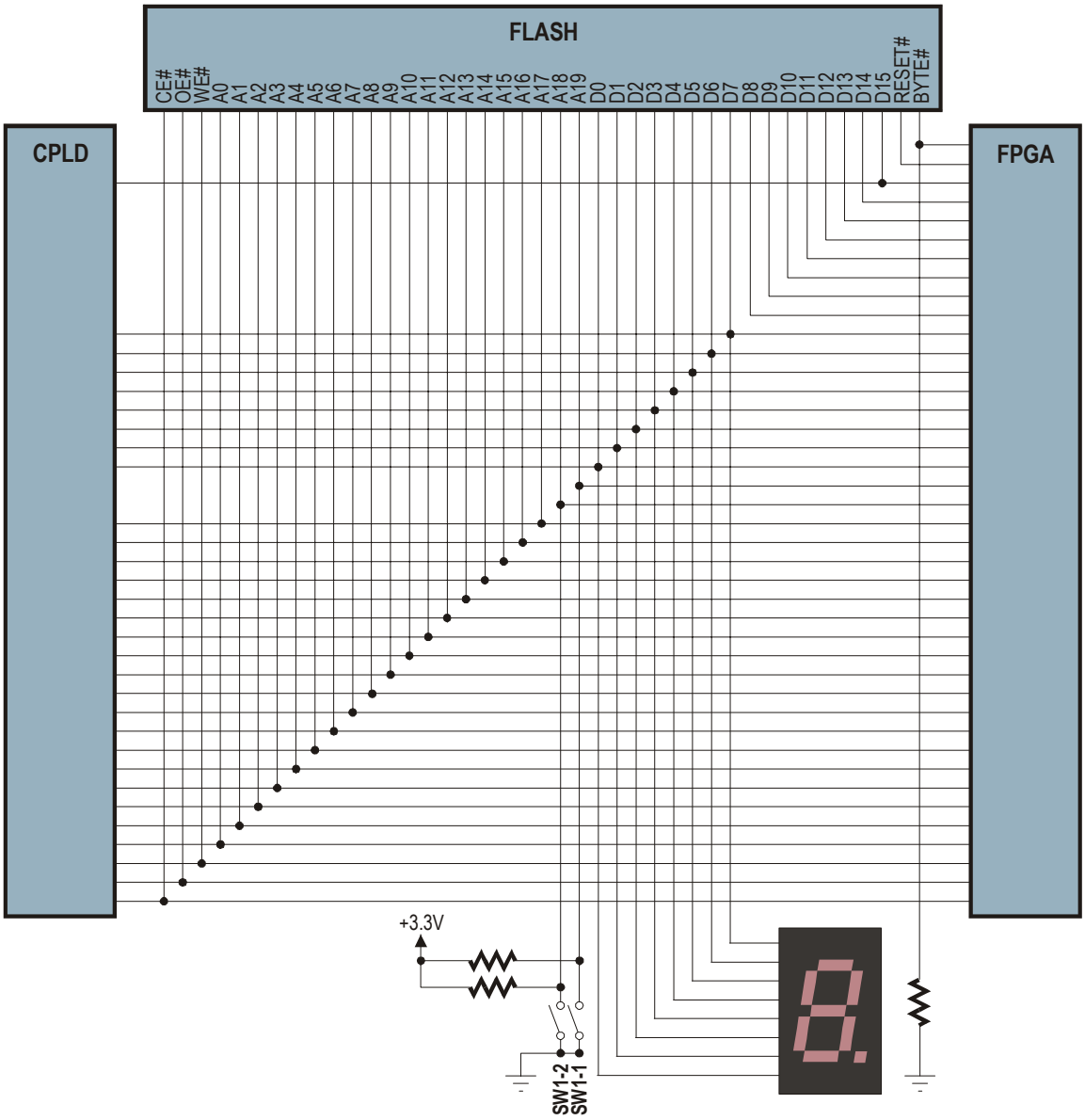

## Flash RAM

The CPLD and FPGA connect to a 16 Mbit Flash RAM (S29AL016M10TAI020) that operates in either byte mode (2M x 8) or word mode (1M x 16). The CPLD uses the byte mode as it only has access to the lower eight bits of the Flash data bus, while the FPGA connects to the entire 16-bit data bus and can select either mode using the BYTE# control line.

The FPGA has access to the entire Flash address bus so it can read or write any location. For this reason, the FPGA is used to pass data between the parallel port and the Flash when GXSLOAD downloads/uploads files to/from the Flash. The CPLD, however, is not connected to the upper two address lines so it can only access a quadrant of the Flash. The quadrant is selected by two DIP switches connected to the upper address lines. On power-up in stand-alone mode, the CPLD configures the FPGA with a bitstream retrieved

from the selected quadrant, so the DIP switches can be used to select between four separate bitstreams stored in the Flash. (See the application note on the XSA Board Flash configuration circuit for more details on this.)

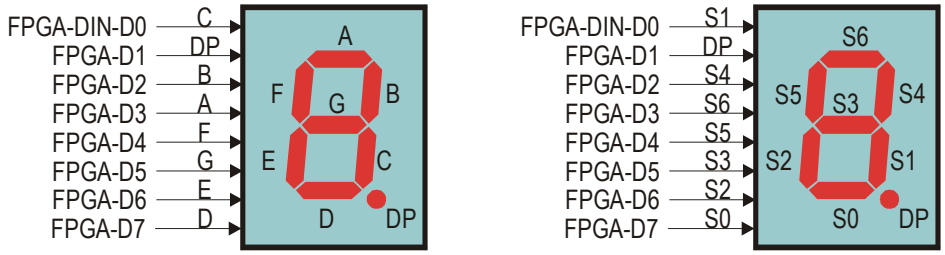
After power-up, any application circuit loaded into the FPGA can read and/or write the Flash. To avoid contention, the CPLD is programmed to release control of all Flash address/data/control lines whenever the FPGA lowers the Flash CE# line. When the Flash is disabled by raising CE#, the I/O lines connected to the Flash are available for general-purpose communication between the FPGA and the CPLD.



## Seven-Segment LED

The XSA-3S1000 Board has a 7-segment LED digit for use by the FPGA or the CPLD. Segments of the LED glow when a logic-high level is applied to them.

The LED shares the same eight-bit data bus that interconnects the CPLD, the FPGA configuration port and the lower-byte of the Flash RAM data bus. The connections between the LED segments and the data bus are shown below. (We use two distinct labelings of the LED segments in our documentation and design examples, so we show the connections for both.)



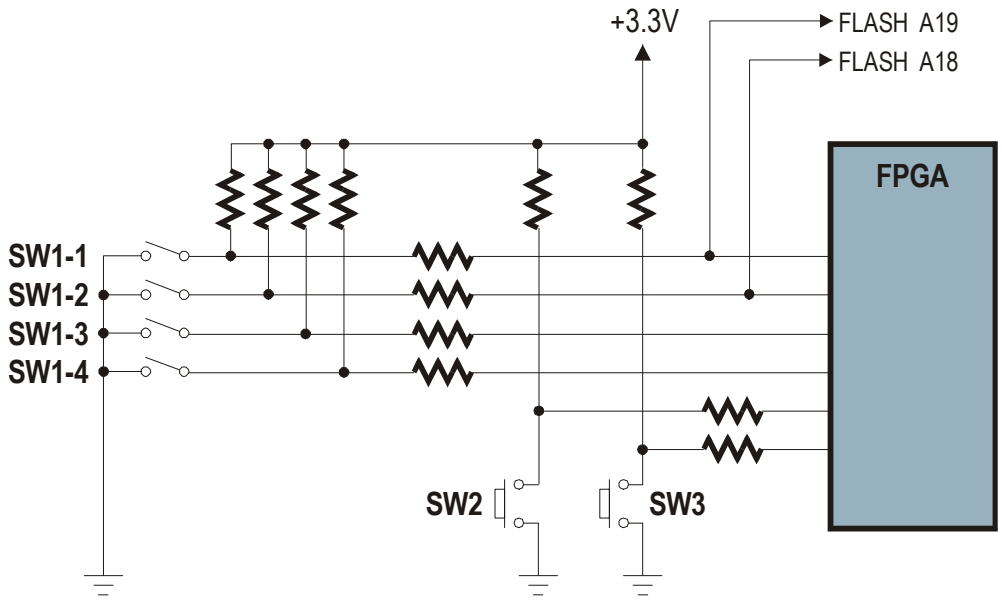

## DIP Switches and Pushbuttons

Four DIP switches are attached to the FPGA. When closed (ON), each switch pulls the connected pin of the FPGA to ground. The pin is pulled high through a resistor when the switch is open (OFF).

Two of the DIP switches also connect to the upper two bits of the Flash address bus. These DIP switches are used to select the Flash quadrant holding a bitstream that will be loaded into the FPGA by the CPLD on power-up.

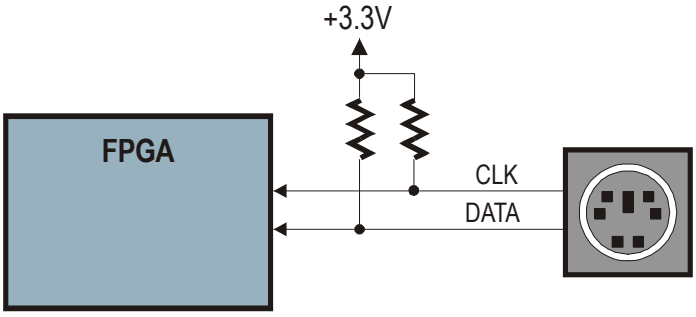
The FPGA also connects to two pushbuttons. Each pushbutton applies a low level to its FPGA pin when pressed and a resistor pulls the pin to a high level when the pushbutton is released.

Small resistors are placed in series between the FPGA and the switches and pushbuttons to prevent damage if the FPGA tries to drive a pin that is being pulled low.




## PS/2 Port

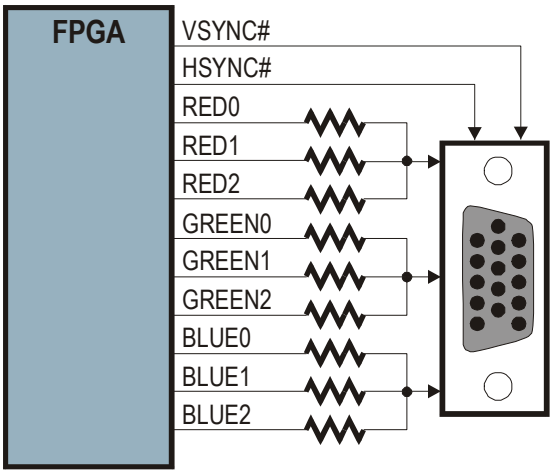
A PS/2 port provides the FPGA with an interface to either a keyboard or a mouse. The FPGA receives two signals from the PS/2 interface: a clock signal and a serial data stream that is synchronized with the falling edge of the clock. (For more details on using the PS/2 port and a simple circuit for receiving keystroke information from a keyboard, see this application note.)




## VGA Port

The FPGA can generate a video signal for display on a VGA monitor. The FPGA outputs three bits each of red, green, and blue color information to a simple resistor-ladder DAC. This provides a palette of $2^3 \times 2^3 \times 2^3 = 512$ colors. The outputs of the DAC are sent to the

RGB inputs of a VGA monitor. The FPGA also generates the horizontal and vertical sync pulses (HSYNC#, VSYNC#). ( See this application note for more details on a simple circuit for generating VGA signals that displays an image stored in SDRAM.)



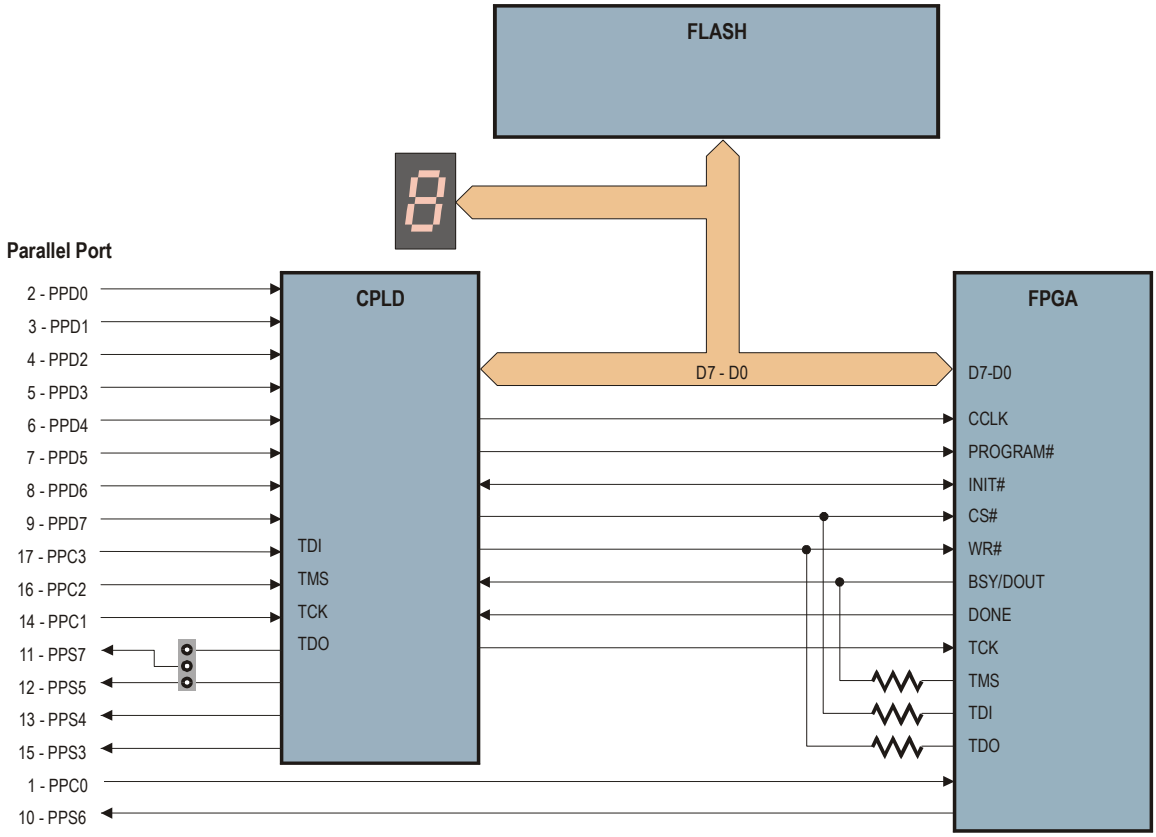

## Parallel Port

The parallel port is the main interface for communicating between the XSA-3S1000 Board and a PC. Control line C0 and status line S6 connect directly to the FPGA and can be used for bidirectional communication between the FPGA and PC. The CPLD handles the fifteen remaining active lines of the parallel port as follows.

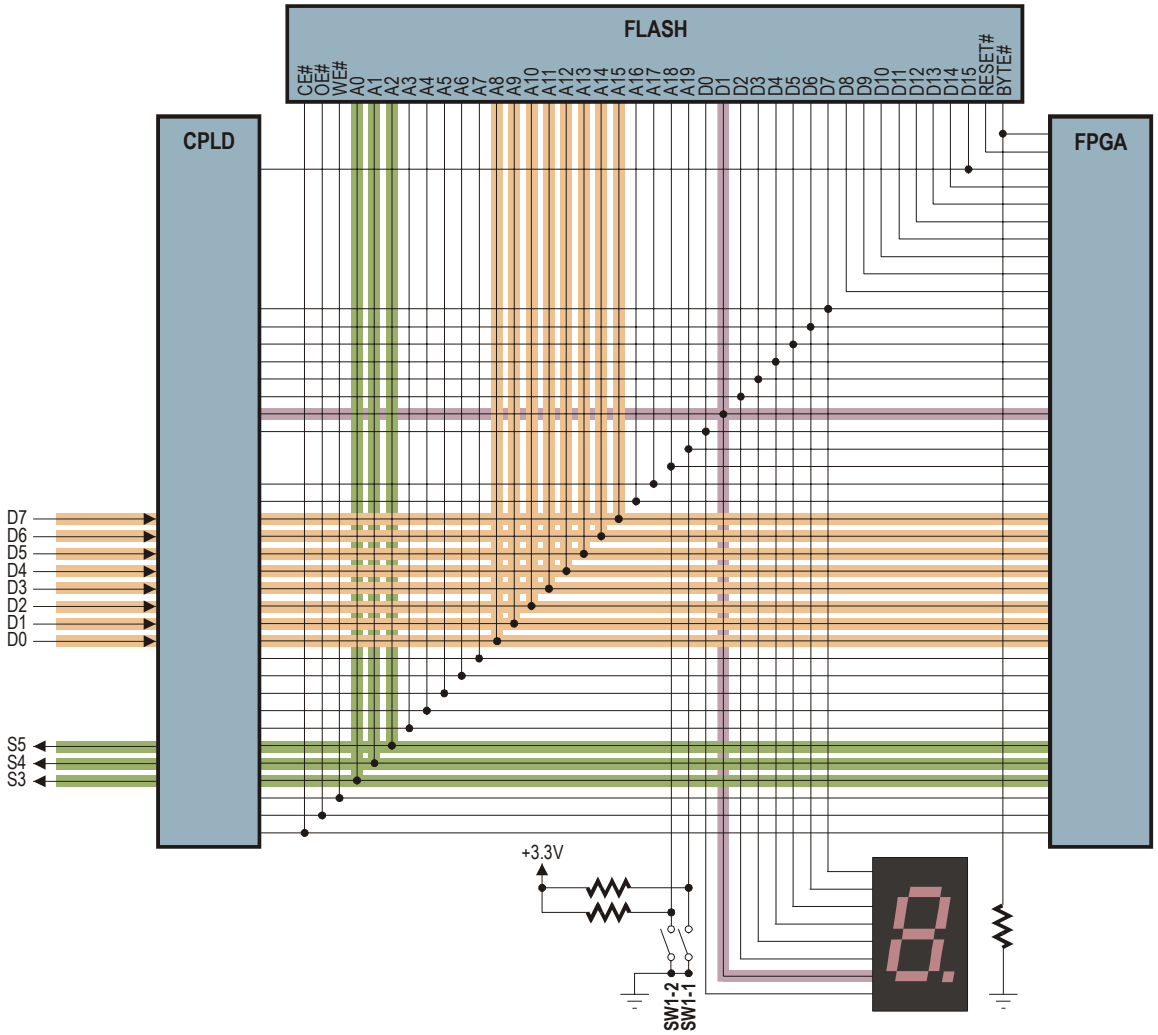
Three of the parallel port control lines, C1–C3, connect to the JTAG pins through which the CPLD is programmed. The C1 control line clocks configuration data presented on the C3 line into the CPLD while the C2 signal steers the actions of the CPLD programming state machine. Meanwhile, information from the CPLD returns to the PC through status line S7.

The eight data lines, D0–D7, and the remaining three status lines, S3–S5, connect to general-purpose pins of the CPLD. The CPLD can be programmed to act as an interface between the FPGA and the parallel port. The CPLD connects to the FPGA configuration pins so it can pass bitstreams from the parallel port to the FPGA. The actual configuration data is presented to the FPGA on the same 8-bit bus that also connects to the Flash and seven-segment LED. The CPLD also drives the configuration pins (CCLK, PROGRAM#, CS#, and WR#) that sequence the loading of a bitstream into the FPGA. The CPLD can monitor the status of the bitstream download through the INIT#, DONE, and BSY/DOUT pins.

The CPLD also has access to the FPGA's JTAG pins: TCK, TMS, TDI, and TDO. The TMS, TDI, and TDO pins share the connections with the BSY/DOUT, CS#, and WR# pins. The CPLD can be programmed with an interface that allows configuration of the FPGA through the JTAG pins using the XILINX iMPACT software (see this application note for more details). Jumper J9 allows the connection of status pin S7 to the general-purpose CPLD pin that also drives status pin S5. This is required by the iMPACT software so it can check for the presence of the downloading cable.




After the FPGA is configured with a bitstream and the DONE pin goes high, the CPLD switches into a mode that connects the parallel port data and status pins to the FPGA. This lets the PC pass data to the FPGA over the parallel port data lines while receiving data from the FPGA over the status lines. The active connections between the FPGA, CPLD and the parallel port after configuration are shown below.




The FPGA sends data to the PC by driving logic levels onto the A0, A1 and A2 Flash address lines which pass through the CPLD and onto the parallel port status lines S3, S4 and S5, respectively. Conversely, the PC sends data to the FPGA on parallel port data lines D7–D0 and the data passes through the CPLD and ends up on the A15–A8 Flash address lines, respectively. The FPGA should never drive A15–A8 unless it is accessing the Flash, otherwise the CPLD and/or FPGA could be damaged. The CPLD can sense when the FPGA lowers the Flash CE# and it will release the Flash address lines so the FPGA can drive them without contention.

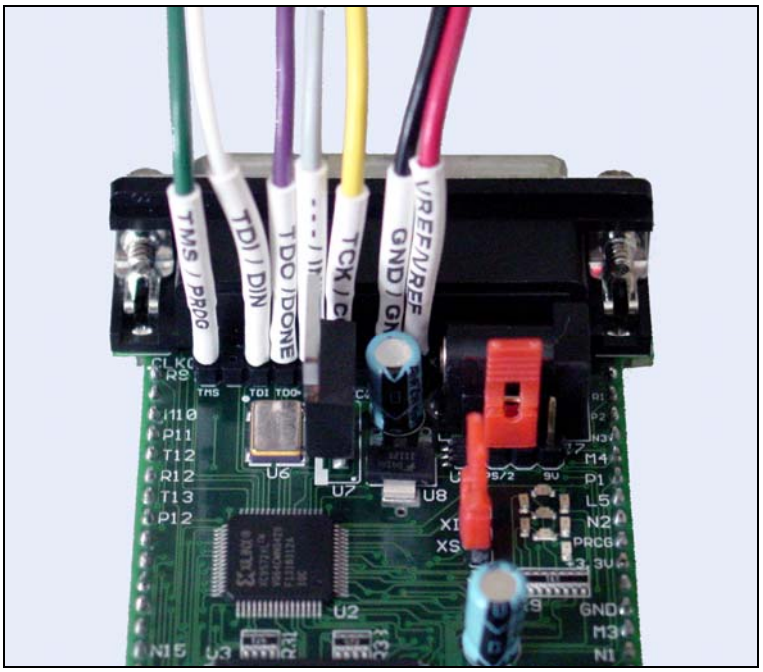
The CPLD also drives the decimal-point of the LED display (connected to Flash data line D1) to give a visual indication when the FPGA is configured with a valid bitstream. Unless it is accessing the Flash RAM, the FPGA should never drive Flash data line D1 to a low logic level or it may damage itself or the CPLD. But when the FPGA lowers the Flash CE#, the CPLD will stop driving the LED decimal-point to allow the FPGA access to data line D1 of the Flash.

For more details on how the CPLD manages the interface between the parallel port and the FPGA both before and after device configuration, see this application note.

## XILINX Parallel Cable IV Connector

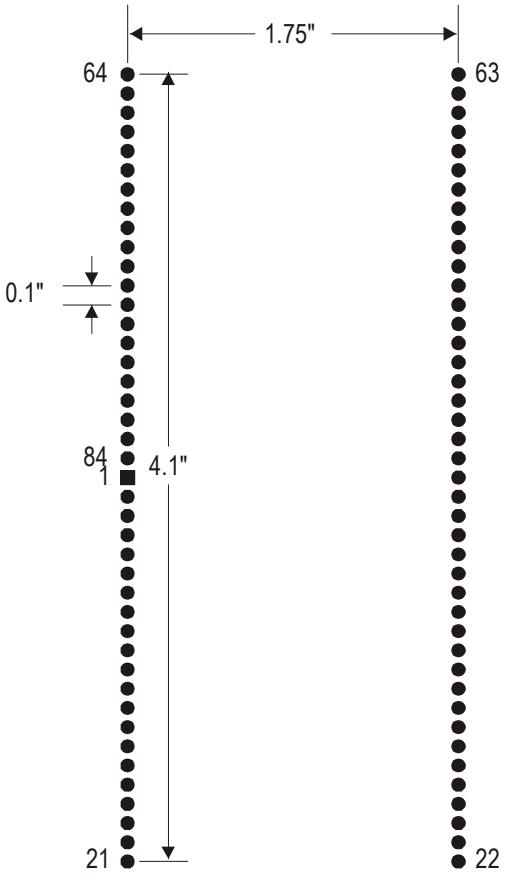
The XSA-3S1000 Board has a connector (X4) for attaching a XILINX Parallel Cable IV. The connections between the Parallel Cable IV and the XSA-3S1000 Board are shown below.

You will need to reprogram the CPLD on the XSA-3S1000 Board with the XSTOOLS\XSA\3S1000\p4jtag.svf file before you can use the Parallel Cable IV. Then disconnect the XESS downloading cable and connect the Parallel Cable IV to the X4 connector. **You should never simultaneously attach a Parallel Cable IV and the XESS parallel port downloading cable!** After connecting the Parallel Cable IV, you can use iMPACT to download bitstreams to the FPGA in boundary-scan mode.




## Prototyping Header

The pins of the FPGA are accessible through the 84-pin prototyping header on the underside of the XSA-3S1000 Board. Pin 1 of the header (denoted by a square pad) is located in the middle of the left-hand edge of the board and the remaining 83 pins are arranged counter-clockwise around the periphery. The physical dimensions of the prototyping header and the pin arrangement are shown below.




A subset of the FPGA pins connects to the prototyping header. These pins are not connected to any of the other components on the XSA-3S1000 Board so they are completely free to use for I/O operations with external systems without any restrictions.

The number of the FPGA pin connected to a given header pin is printed next to the header pin on the board. This makes it easier to find a given FPGA pin when you want to connect it to an external system.

# A

# XSA-3S1000 Pin Connections

The following tables list the pin numbers of the FPGA and CPLD along with the pin names of the other chips that they connect to on the XSA-3S1000 Board.

| Connections Between the FPGA, CPLD and other Components on the XSA-3S1000 Board | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Net Name** | **FPGA Pin (U1)** | **CPLD Pin (U2)** | **Parallel Port** | **LEDs** | **Switch / Buttons** | **SDRAM (U4)** | **Flash (U3)** | **Osc (U6)** | **VGA** | **PS/2** | **Proto. Pin (J1)** |
| +1.2V | D4,D13,E5,E12,M5,M12,N4,N13 | | | | | | | | | | |
| +2.5V | C4,T2,P4,A6,A11,F1,F16,L1,L16,T6,T11 | | | | | | | | | | 22 |
| +3.3V | E8,F7,F8,E9,F9,F10,G11,H11,H | 3,37,26,55 | | | | VDD (1,3,9,1 | VCC (37) | VCC (4) | | | 54 |
| +5V | | | | | | | | | | | 2 |
| CLKA | T9 | 60 | | | | | | | | | |
| CLKB | P8 | 61 | | | | | | | | | 11 |
| CLKC | R9 | | | | | | | | | | 64 |
| CPLD-TDO | | 53 | | | | | | | | | |
| FLASH-A0 | N5 | 62 | | | | | A0 (25) | | | | |
| FLASH-A1 | K14 | 51 | | | | | A1 (24) | | | | |
| FLASH-A2 | K13 | 50 | | | | | A2 (23) | | | | |
| FLASH-A3 | K12 | 49 | | | | | A3 (22) | | | | |
| FLASH-A4 | L14 | 48 | | | | | A4 (21) | | | | |
| FLASH-A5 | M16 | 47 | | | | | A5 (20) | | | | |
| FLASH-A6 | L13 | 46 | | | | | A6 (19) | | | | |
| FLASH-A7 | N16 | 45 | | | | | A7 (18) | | | | |
| FLASH-A8 | N14 | 40 | | | | | A8 (8) | | | | |
| FLASH-A9 | P15 | 39 | | | | | A9 (7) | | | | |
| FLASH-A10 | R16 | 38 | | | | | A10 (6) | | | | |
| FLASH-A11 | P14 | 36 | | | | | A11 (5) | | | | |
| FLASH-A12 | P13 | 35 | | | | | A12 (4) | | | | |
| FLASH-A13 | N12 | 34 | | | | | A13 (3) | | | | |
| FLASH-A14 | T14 | 33 | | | | | A14 (2) | | | | |
| FLASH-A15 | R13 | 32 | | | | | A15 (1) | | | | |
| FLASH-A16 | N10 | 13 | | | | | A16 (48) | | | | |
| FLASH-A17 | M14 | 44 | | | | | A17 (17) | | | | |
| FLASH-A18 | K3 | | | | SW1-2 | | A18 (16) | | | | |
| FLASH-A19 | K4 | | | | SW1-1 | | A19 (9) | | | | |
| FLASH-BYTE# | T8 | | | | | | BYTE# (47) | | | | |
| FLASH-CE# | R4 | 63 | | | | | CE# (26) | | | | |
| FLASH-D8 | T4 | | | | | | DQ8 (30) | | | | |
| FLASH-D9 | R5 | | | | | | DQ9 (32) | | | | |
| FLASH-D10 | T5 | | | | | | DQ10 (34) | | | | |
| FLASH-D11 | P6 | | | | | | DQ11 (36) | | | | |
| FLASH-D12 | M7 | | | | | | DQ12 (39) | | | | |
| FLASH-D13 | R6 | | | | | | DQ13 (41) | | | | |
| FLASH-D14 | N7 | | | | | | DQ14 (43) | | | | |
| FLASH-D15 | P7 | 12 | | | | | DQ15/A-1 (45) | | | | |
| FLASH-OE# | P5 | 64 | | | | | OE# (28) | | | | |
| FLASH-RDY | L12 | | | | | | RY/BY# (15) | | | | |
| FLASH-RESET# | P16 | | | | | | RESET# (12) | | | | |
| FLASH-WE# | M13 | 42 | | | | | WE# (11) | | | | |
| FPGA-CCLK | T15 | 52 | | | | | | | | | |
| FPGA-DIN-D0 | M11 | 1 | | LED-C (S1) | | | DQ0 (29) | | | | |
| FPGA-D1 | N11 | 2 | | LED-DP | | | DQ1 (31) | | | | |
| FPGA-D2 | P10 | 4 | | LED-B (S4) | | | DQ2 (33) | | | | |
| FPGA-D3 | R10 | 5 | | LED-A (S6) | | | DQ3 (35) | | | | |
| FPGA-D4 | T7 | 7 | | LED-F (S5) | | | DQ4 (38) | | | | |
| FPGA-D5 | R7 | 9 | | LED-G (S3) | | | DQ5 (40) | | | | |
| FPGA-D6 | N6 | 10 | | LED-E (S2) | | | DQ6 (42) | | | | |
| FPGA-D7 | M6 | 11 | | LED-D (S0) | | | DQ7 (44) | | | | |
| FPGA-DONE | R14 | 6 | | | | | | | | | |
| FPGA-INIT# | N9 | 8 | | | | | | | | | |

| Connections Between the FPGA, CPLD and other Components on the XSA-3S1000 Board | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Net Name | FPGA Pin (U1) | CPLD Pin (U2) | Parallel Port | LEDs | Switch / Buttons | SDRAM (U4) | Flash (U3) | Osc (U6) | VGA | PS/2 | Proto. Pin (J1) |
| FPGA-PROG# | B3 | 57 | | | | | | | | | 55 |
| FPGA-TCK | C14 | 43 | | | | | | | | | 16 |
| FPGA-TDI | A2 | | | | | | | | | | |
| FPGA-TDI-CS# | R3 | 58 | | | | | | | | | 15 |
| FPGA-TDO | A15 | | | | | | | | | | |
| FPGA-TDO-WR# | T3 | 56 | | | | | | | | | 30 |
| FPGA-TMS | C13 | | | | | | | | | | |
| FPGA-TMS-BSY | P9 | 59 | | | | | | | | | 17 |
| GND | P3,A1,A16,B2,B9,B15,F6,F11,G | 14,21,41,54 | | GND (U5.4, U5.12) | | VSS (6,12,4 | VSS (27,46) | GND(2) | | | 52 |
| MASTER-CLK | | 17 | | | | | | OUT (3) | | | |
| PP-C0 | R11 | | C0 (1) | | | | | | | | |
| PP-C1 | | 30 | C1 (14) | | | | | | | | |
| PP-C2 | | 29 | C2 (16) | | | | | | | | |
| PP-C3 | | 28 | C3 (17) | | | | | | | | |
| PP-D0 | | 27 | D0 (2) | | | | | | | | |
| PP-D1 | | 20 | D1 (3) | | | | | | | | |
| PP-D2 | | 31 | D2 (4) | | | | | | | | |
| PP-D3 | | 23 | D3 (5) | | | | | | | | |
| PP-D4 | | 22 | D4 (6) | | | | | | | | |
| PP-D5 | | 19 | D5 (7) | | | | | | | | |
| PP-D6 | | 18 | D6 (8) | | | | | | | | |
| PP-D7 | | 16 | D7 (9) | | | | | | | | |
| PP-S3 | | 24 | S3 (15) | | | | | | | | |
| PP-S4 | | 25 | S4 (13) | | | | | | | | |
| PP-S5 | | 15 | S5 (12) | | | | | | | | |
| PP-S6 | T10 | | S6 (10) | | | | | | | | |
| PP-S7 | | | S7 (11) | | | | | | | | |
| PROTO1 | H16 | | | | | | | | | | 1 |
| PROTO3 | H15 | | | | | | | | | | 3 |
| PROTO4 | H14 | | | | | | | | | | 4 |
| PROTO5 | H13 | | | | | | | | | | 5 |
| PROTO6 | G16 | | | | | | | | | | 6 |
| PROTO7 | G15 | | | | | | | | | | 7 |
| PROTO8 | G14 | | | | | | | | | | 8 |
| PROTO9 | G13 | | | | | | | | | | 9 |
| PROTO10 | F15 | | | | | | | | | | 10 |
| PROTO12 | G12 | | | | | | | | | | 12 |
| PROTO13 | F14 | | | | | | | | | | 13 |
| PROTO14 | E16 | | | | | | | | | | 14 |
| PROTO18 | E15 | | | | | | | | | | 18 |
| PROTO19 | D16 | | | | | | | | | | 19 |
| PROTO20 | E14 | | | | | | | | | | 20 |
| PROTO21 | D15 | | | | | | | | | | 21 |
| PROTO23 | F5 | | | | | | | | | | 23 |
| PROTO24 | D2 | | | | | | | | | | 24 |
| PROTO25 | D1 | | | | | | | | | | 25 |
| PROTO26 | F4 | | | | | | | | | | 26 |
| PROTO27 | E2 | | | | | | | | | | 27 |
| PROTO28 | E1 | | | | | | | | | | 28 |
| PROTO29 | F3 | | | | | | | | | | 29 |
| PROTO31 | G5 | | | | | | | | | | 31 |
| PROTO32 | F2 | | | | | | | | | | 32 |
| PROTO33 | G4 | | | | | | | | | | 33 |

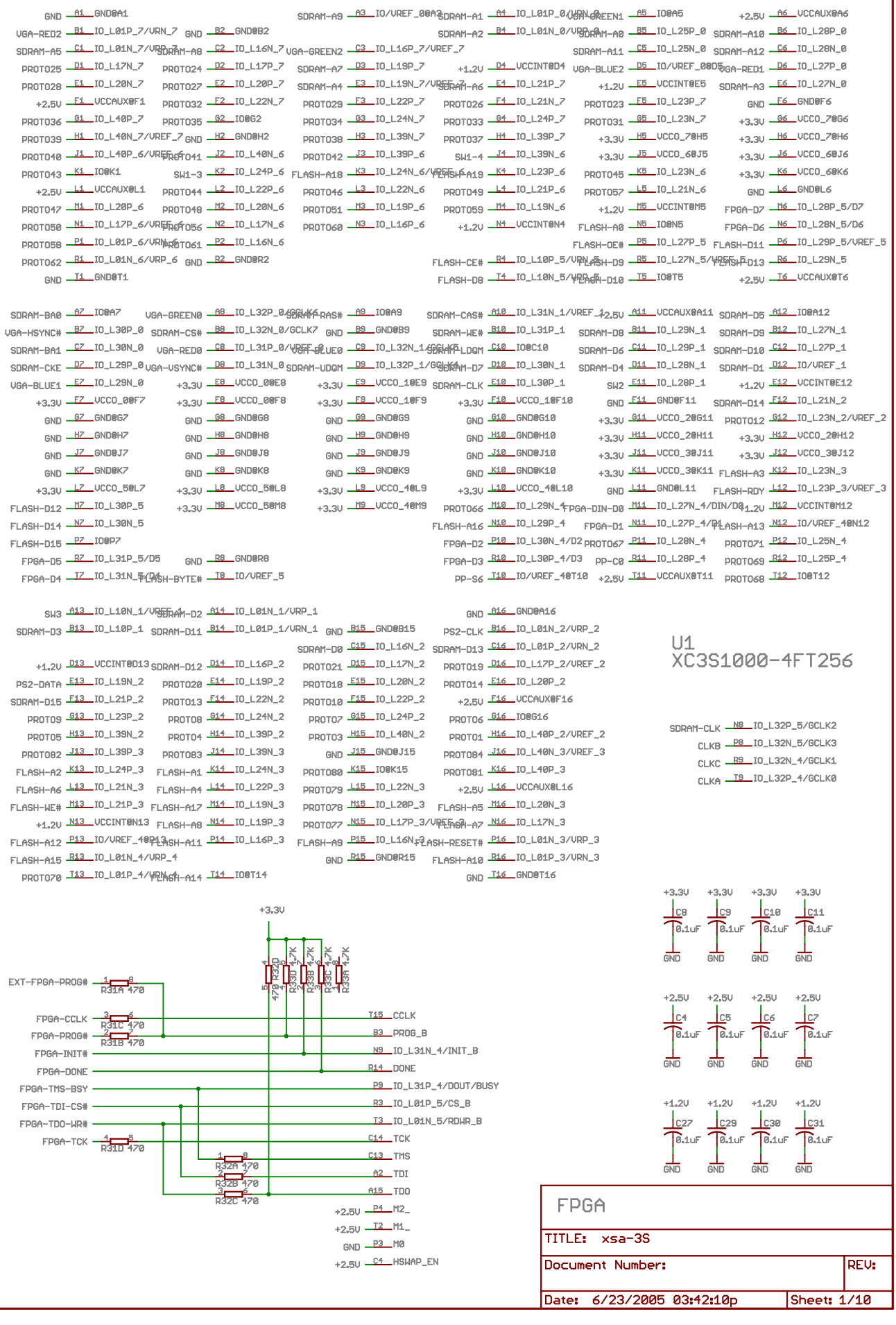
| Connections Between the FPGA, CPLD and other Components on the XSA-3S1000 Board | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Net Name | FPGA Pin (U1) | CPLD Pin (U2) | Parallel Port | LEDs | Switch / Buttons | SDRAM (U4) | Flash (U3) | Osc (U6) | VGA | PS/2 | Proto. Pin (J1) |
| PROTO34 | G3 | | | | | | | | | | 34 |
| PROTO35 | G2 | | | | | | | | | | 35 |
| PROTO36 | G1 | | | | | | | | | | 36 |
| PROTO37 | H4 | | | | | | | | | | 37 |
| PROTO38 | H3 | | | | | | | | | | 38 |
| PROTO39 | H1 | | | | | | | | | | 39 |
| PROTO40 | J1 | | | | | | | | | | 40 |
| PROTO41 | J2 | | | | | | | | | | 41 |
| PROTO42 | J3 | | | | | | | | | | 42 |
| PROTO43 | K1 | | | | | | | | | | 43 |
| PROTO44 | L2 | | | | | | | | | | 44 |
| PROTO45 | K5 | | | | | | | | | | 45 |
| PROTO46 | L3 | | | | | | | | | | 46 |
| PROTO47 | M1 | | | | | | | | | | 47 |
| PROTO48 | M2 | | | | | | | | | | 48 |
| PROTO49 | L4 | | | | | | | | | | 49 |
| PROTO50 | N1 | | | | | | | | | | 50 |
| PROTO51 | M3 | | | | | | | | | | 51 |
| PROTO53 | | | | | | | | | | | 53 |
| PROTO56 | N2 | | | | | | | | | | 56 |
| PROTO57 | L5 | | | | | | | | | | 57 |
| PROTO58 | P1 | | | | | | | | | | 58 |
| PROTO59 | M4 | | | | | | | | | | 59 |
| PROTO60 | N3 | | | | | | | | | | 60 |
| PROTO61 | P2 | | | | | | | | | | 61 |
| PROTO62 | R1 | | | | | | | | | | 62 |
| PROTO63 | | | | | | | | | | | 63 |
| PROTO65 | | | | | | | | | | | 65 |
| PROTO66 | M10 | | | | | | | | | | 66 |
| PROTO67 | P11 | | | | | | | | | | 67 |
| PROTO68 | T12 | | | | | | | | | | 68 |
| PROTO69 | R12 | | | | | | | | | | 69 |
| PROTO70 | T13 | | | | | | | | | | 70 |
| PROTO71 | P12 | | | | | | | | | | 71 |
| PROTO72 | | | | | | | | | | | 72 |
| PROTO73 | | | | | | | | | | | 73 |
| PROTO74 | | | | | | | | | | | 74 |
| PROTO75 | | | | | | | | | | | 75 |
| PROTO76 | | | | | | | | | | | 76 |
| PROTO77 | N15 | | | | | | | | | | 77 |
| PROTO78 | M15 | | | | | | | | | | 78 |
| PROTO79 | L15 | | | | | | | | | | 79 |
| PROTO80 | K15 | | | | | | | | | | 80 |
| PROTO81 | K16 | | | | | | | | | | 81 |
| PROTO82 | J13 | | | | | | | | | | 82 |
| PROTO83 | J14 | | | | | | | | | | 83 |
| PROTO84 | J16 | | | | | | | | | | 84 |
| PS2-CLK | B16 | | | | | | | | | CLK (5) | |
| PS2-DATA | E13 | | | | | | | | | DATA (1) | |
| SDRAM-A0 | B5 | | | | | A0 (23) | | | | | |
| SDRAM-A1 | A4 | | | | | A1 (24) | | | | | |
| SDRAM-A2 | B4 | | | | | A2 (25) | | | | | |
| SDRAM-A3 | E6 | | | | | A3 (26) | | | | | |

| Connections Between the FPGA, CPLD and other Components on the XSA-3S1000 Board | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Net Name | FPGA Pin (U1) | CPLD Pin (U2) | Parallel Port | LEDs | Switch / Buttons | SDRAM (U4) | Flash (U3) | Osc (U6) | VGA | PS/2 | Proto. Pin (J1) |
| SDRAM-A4 | E3 | | | | | A4 (29) | | | | | |
| SDRAM-A5 | C1 | | | | | A5 (30) | | | | | |
| SDRAM-A6 | E4 | | | | | A6 (31) | | | | | |
| SDRAM-A7 | D3 | | | | | A7 (32) | | | | | |
| SDRAM-A8 | C2 | | | | | A8 (33) | | | | | |
| SDRAM-A9 | A3 | | | | | A9 (34) | | | | | |
| SDRAM-A10 | B6 | | | | | A10 (22) | | | | | |
| SDRAM-A11 | C5 | | | | | A11 (35) | | | | | |
| SDRAM-A12 | C6 | | | | | A12 (36) | | | | | |
| SDRAM-BA0 | A7 | | | | | BA0 (20) | | | | | |
| SDRAM-BA1 | C7 | | | | | BA1 (21) | | | | | |
| SDRAM-CAS# | A10 | | | | | CAS# (17) | | | | | |
| SDRAM-CKE | D7 | | | | | CKE (37) | | | | | |
| SDRAM-CLK | N8 | | | | | CLK (38) | | | | | |
| SDRAM-CLK | E10 | | | | | | | | | | |
| SDRAM-CS# | B8 | | | | | CS# (19) | | | | | |
| SDRAM-D0 | C15 | | | | | DQ0 (2) | | | | | |
| SDRAM-D1 | D12 | | | | | DQ1 (4) | | | | | |
| SDRAM-D2 | A14 | | | | | DQ2 (5) | | | | | |
| SDRAM-D3 | B13 | | | | | DQ3 (7) | | | | | |
| SDRAM-D4 | D11 | | | | | DQ4 (8) | | | | | |
| SDRAM-D5 | A12 | | | | | DQ5 (10) | | | | | |
| SDRAM-D6 | C11 | | | | | DQ6 (11) | | | | | |
| SDRAM-D7 | D10 | | | | | DQ7 (13) | | | | | |
| SDRAM-D8 | B11 | | | | | DQ8 (42) | | | | | |
| SDRAM-D9 | B12 | | | | | DQ9 (44) | | | | | |
| SDRAM-D10 | C12 | | | | | DQ10 (45) | | | | | |
| SDRAM-D11 | B14 | | | | | DQ11 (47) | | | | | |
| SDRAM-D12 | D14 | | | | | DQ12 (48) | | | | | |
| SDRAM-D13 | C16 | | | | | DQ13 (50) | | | | | |
| SDRAM-D14 | F12 | | | | | DQ14 (51) | | | | | |
| SDRAM-D15 | F13 | | | | | DQ15 (53) | | | | | |
| SDRAM-LDQM | C10 | | | | | LDQM (15) | | | | | |
| SDRAM-RAS# | A9 | | | | | RAS# (18) | | | | | |
| SDRAM-UDQM | D9 | | | | | UDQM (39) | | | | | |
| SDRAM-WE# | B10 | | | | | WE# (16) | | | | | |
| SW1-3 | K2 | | | | SW1-3 | | | | | | |
| SW1-4 | J4 | | | | SW1-4 | | | | | | |
| SW2 | E11 | | | | SW2 | | | | | | |
| SW3 | A13 | | | | SW3 | | | | | | |
| VGA-BLUE0 | C9 | | | | | | | | BLU0 | | |
| VGA-BLUE1 | E7 | | | | | | | | BLU1 | | |
| VGA-BLUE2 | D5 | | | | | | | | BLU2 | | |
| VGA-GREEN0 | A8 | | | | | | | | GRN0 | | |
| VGA-GREEN1 | A5 | | | | | | | | GRN1 | | |
| VGA-GREEN2 | C3 | | | | | | | | GRN2 | | |
| VGA-RED0 | C8 | | | | | | | | RED0 | | |
| VGA-RED1 | D6 | | | | | | | | RED1 | | |
| VGA-RED2 | B1 | | | | | | | | RED2 | | |
| VGA-HSYNC# | B7 | | | | | | | | HSYNC# | | |
| VGA-VSYNC# | D8 | | | | | | | | VSYNC# | | |

# B

# XSA-3S1000 Schematics

The following pages show the detailed schematics for the XSA-3S1000 Board.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FPGA
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REV:
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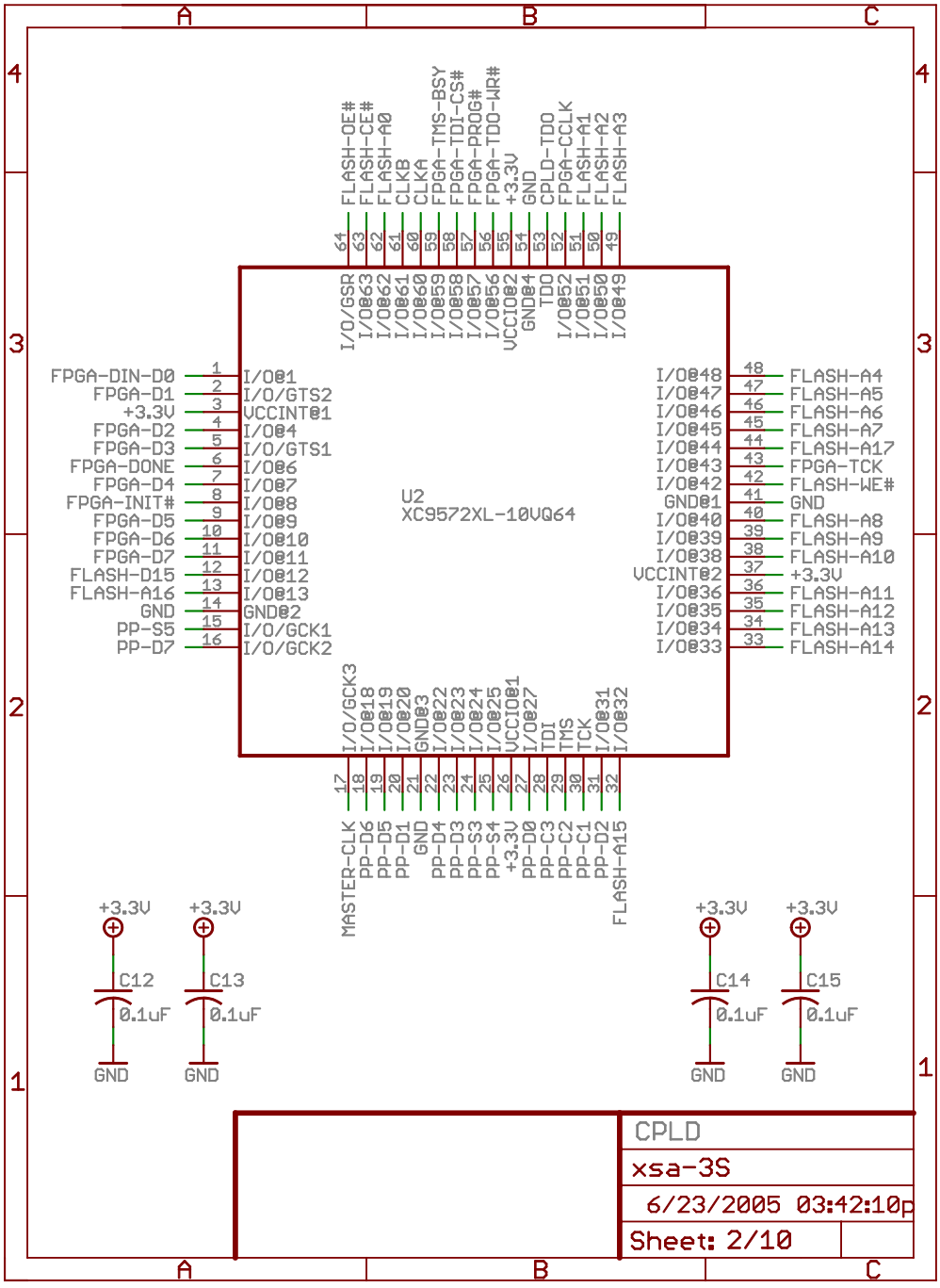
A
B
C
1
2
3
4
U2
XC9572XL-10VQ64
I/O/GSR
I/O@63
I/O@62
I/O@61
I/O@60
I/O@59
I/O@58
I/O@57
I/O@56
VCCIO@2
GND@4
TDO
I/O@52
I/O@51
I/O@50
I/O@49
FLASH-OE#
FLASH-CE#
FLASH-A0
CLKB
CLKA
FPGA-TMS-BSY
FPGA-TDI-CS#
FPGA-PROG#
FPGA-TDO-WR#
+3.3V
GND
CPLD-TDO
FPGA-CCLK
FLASH-A1
FLASH-A2
FLASH-A3
64
63
62
61
60
59
58
57
56
55
54
53
52
51
50
49
FPGA-DIN-D0
FPGA-D1
+3.3V
FPGA-D2
FPGA-D3
FPGA-DONE
FPGA-D4
FPGA-INIT#
FPGA-D5
FPGA-D6
FPGA-D7
FLASH-D15
FLASH-A16
GND
PP-S5
PP-D7
I/O@1
I/O/GTS2
VCCINT@1
I/O@4
I/O/GTS1
I/O@6
I/O@7
I/O@8
I/O@9
I/O@10
I/O@11
I/O@12
I/O@13
GND@2
I/O/GCK1
I/O/GCK2
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
I/O@48
I/O@47
I/O@46
I/O@45
I/O@44
I/O@43
I/O@42
GND@1
I/O@40
I/O@39
I/O@38
VCCINT@2
I/O@36
I/O@35
I/O@34
I/O@33
FLASH-A4
FLASH-A5
FLASH-A6
FLASH-A7
FLASH-A17
FPGA-TCK
FLASH-WE#
GND
FLASH-A8
FLASH-A9
FLASH-A10
+3.3V
FLASH-A11
FLASH-A12
FLASH-A13
FLASH-A14
48
47
46
45
44
43
42
41
40
39
38
37
36
35
34
33
I/O/GCK3
I/O@18
I/O@19
I/O@20
GND@3
I/O@22
I/O@23
I/O@24
I/O@25
VCCIO@1
I/O@27
TDI
TMS
TCK
I/O@31
I/O@32
MASTER-CLK
PP-D6
PP-D5
PP-D1
GND
PP-D4
PP-D3
PP-S3
PP-S4
+3.3V
PP-D0
PP-C3
PP-C2
PP-C1
PP-D2
FLASH-A15
17
18
19
20
21
22
23
24
25
26
27
28
29
30
31
32
+3.3V
+3.3V
C12
0.1uF
GND
C13
0.1uF
GND
+3.3V
+3.3V
C14
0.1uF
GND
C15
0.1uF
GND
CPLD
xsa-3S
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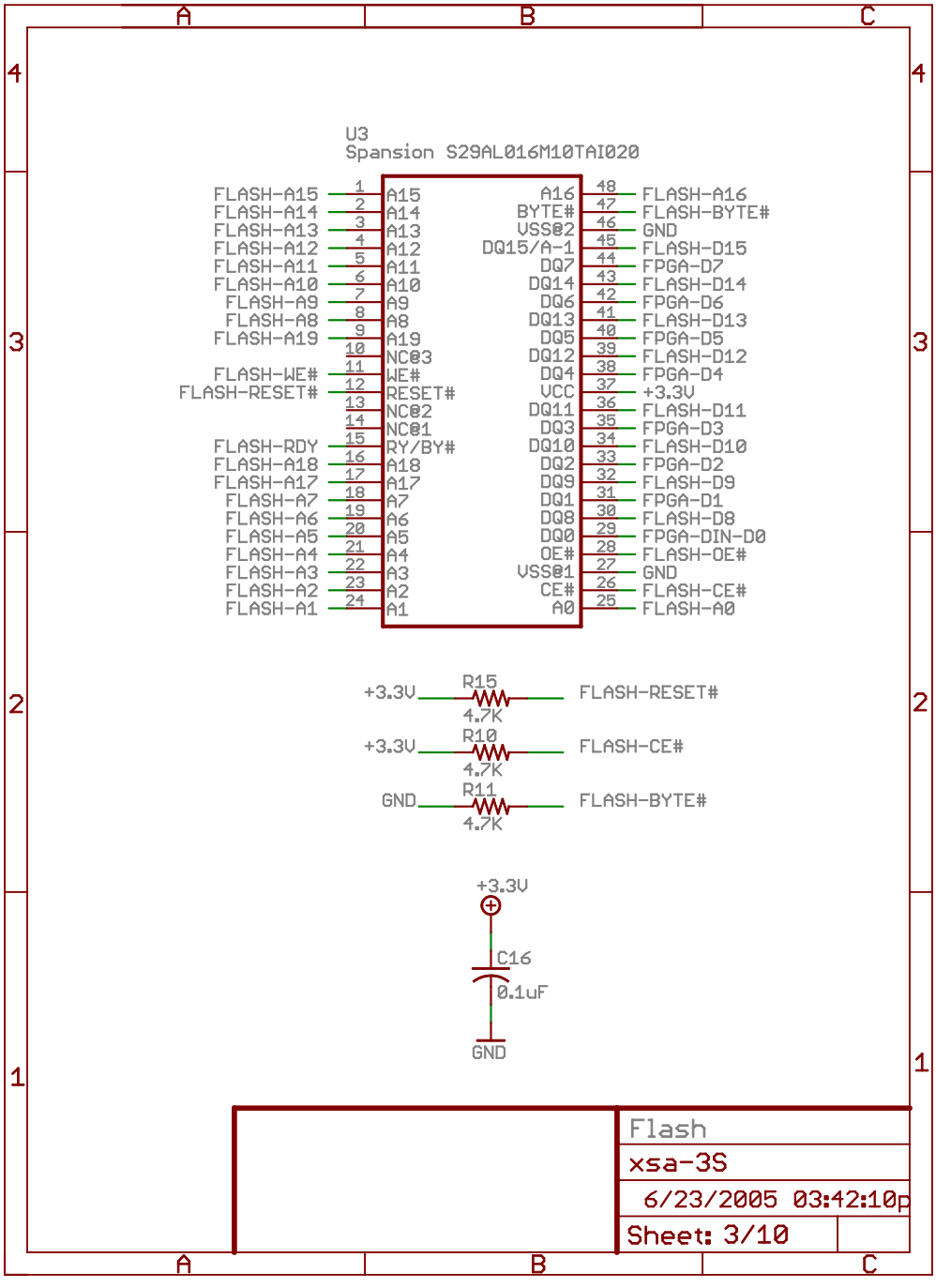
Sheet: 2/10


A
B
C
4
3
2
1
U3
Spansion S29AL016M10TAI020
FLASH-A15 1 A15
FLASH-A14 2 A14
FLASH-A13 3 A13
FLASH-A12 4 A12
FLASH-A11 5 A11
FLASH-A10 6 A10
FLASH-A9 7 A9
FLASH-A8 8 A8
FLASH-A19 9 A19
10 NC@3
FLASH-WE# 11 WE#
FLASH-RESET# 12 RESET#
13 NC@2
14 NC@1
FLASH-RDY 15 RY/BY#
FLASH-A18 16 A18
FLASH-A17 17 A17
FLASH-A7 18 A7
FLASH-A6 19 A6
FLASH-A5 20 A5
FLASH-A4 21 A4
FLASH-A3 22 A3
FLASH-A2 23 A2
FLASH-A1 24 A1
A16 48 FLASH-A16
BYTE# 47 FLASH-BYTE#
VSS@2 46 GND
DQ15/A-1 45 FLASH-D15
DQ7 44 FPGA-D7
DQ14 43 FLASH-D14
DQ6 42 FPGA-D6
DQ13 41 FLASH-D13
DQ5 40 FPGA-D5
DQ12 39 FLASH-D12
DQ4 38 FPGA-D4
VCC 37 +3.3V
DQ11 36 FLASH-D11
DQ3 35 FPGA-D3
DQ10 34 FLASH-D10
DQ2 33 FPGA-D2
DQ9 32 FLASH-D9
DQ1 31 FPGA-D1
DQ8 30 FLASH-D8
DQ0 29 FPGA-DIN-D0
OE# 28 FLASH-OE#
VSS@1 27 GND
CE# 26 FLASH-CE#
A0 25 FLASH-A0
+3.3V
R15
4.7K
FLASH-RESET#
+3.3V
R10
4.7K
FLASH-CE#
GND
R11
4.7K
FLASH-BYTE#
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C16
0.1uF
GND
Flash
xsa-3S
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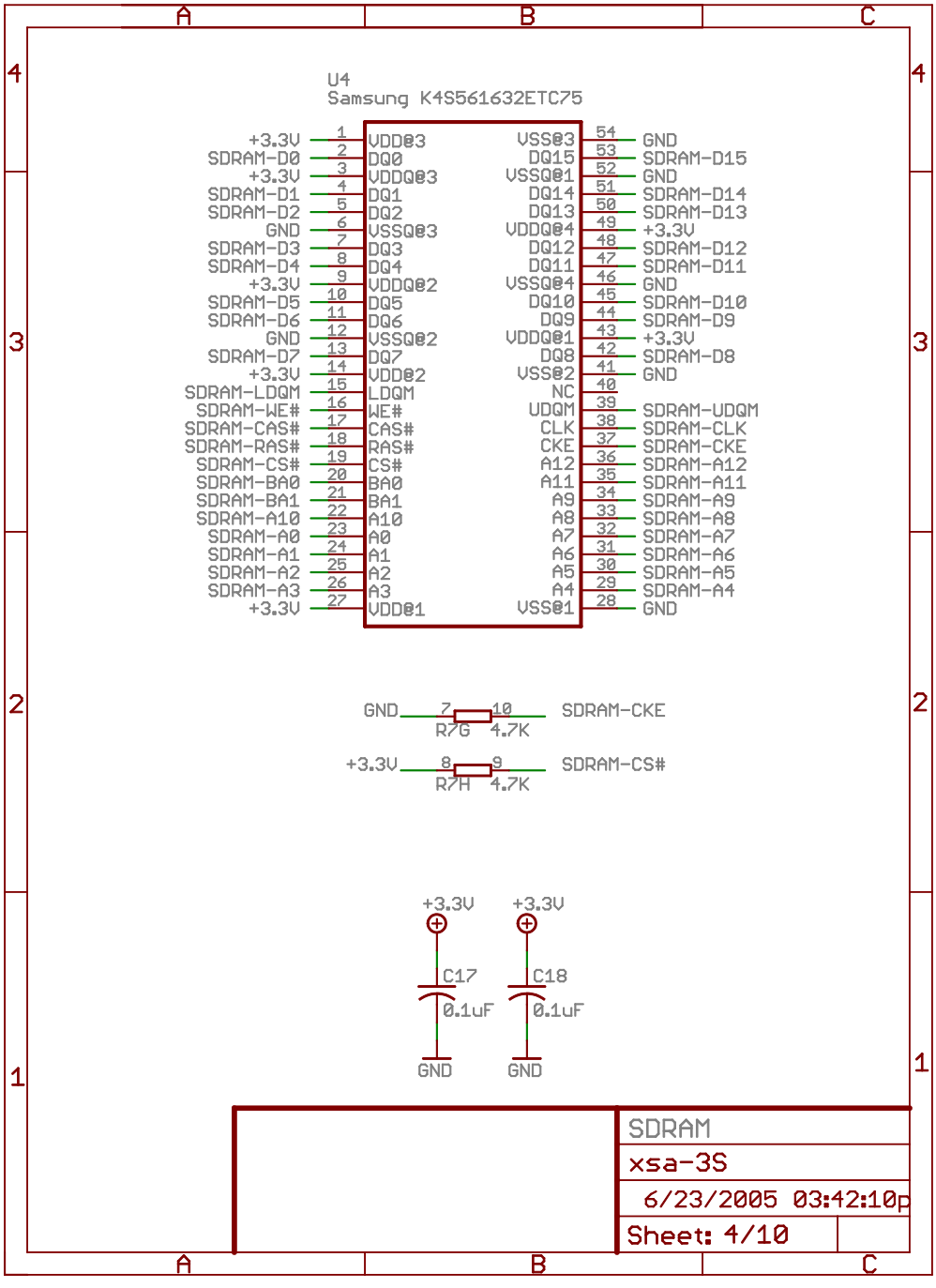
Sheet: 3/10


A
B
C
4
3
2
1
U4
Samsung K4S561632ETC75
+3.3V 1 VDD@3
SDRAM-D0 2 DQ0
+3.3V 3 VDDQ@3
SDRAM-D1 4 DQ1
SDRAM-D2 5 DQ2
GND 6 VSSQ@3
SDRAM-D3 7 DQ3
SDRAM-D4 8 DQ4
+3.3V 9 VDDQ@2
SDRAM-D5 10 DQ5
SDRAM-D6 11 DQ6
GND 12 VSSQ@2
SDRAM-D7 13 DQ7
+3.3V 14 VDD@2
SDRAM-LDQM 15 LDQM
SDRAM-WE# 16 WE#
SDRAM-CAS# 17 CAS#
SDRAM-RAS# 18 RAS#
SDRAM-CS# 19 CS#
SDRAM-BA0 20 BA0
SDRAM-BA1 21 BA1
SDRAM-A10 22 A10
SDRAM-A0 23 A0
SDRAM-A1 24 A1
SDRAM-A2 25 A2
SDRAM-A3 26 A3
+3.3V 27 VDD@1
VSS@3 54 GND
DQ15 53 SDRAM-D15
VSSQ@1 52 GND
DQ14 51 SDRAM-D14
DQ13 50 SDRAM-D13
VDDQ@4 49 +3.3V
DQ12 48 SDRAM-D12
DQ11 47 SDRAM-D11
VSSQ@4 46 GND
DQ10 45 SDRAM-D10
DQ9 44 SDRAM-D9
VDDQ@1 43 +3.3V
DQ8 42 SDRAM-D8
VSS@2 41 GND
NC 40
UDQM 39 SDRAM-UDQM
CLK 38 SDRAM-CLK
CKE 37 SDRAM-CKE
A12 36 SDRAM-A12
A11 35 SDRAM-A11
A9 34 SDRAM-A9
A8 33 SDRAM-A8
A7 32 SDRAM-A7
A6 31 SDRAM-A6
A5 30 SDRAM-A5
A4 29 SDRAM-A4
VSS@1 28 GND
GND 7 R7G 10 SDRAM-CKE
4.7K
+3.3V 8 R7H 9 SDRAM-CS#
4.7K
+3.3V
C17
0.1uF
GND
+3.3V
C18
0.1uF
GND
SDRAM
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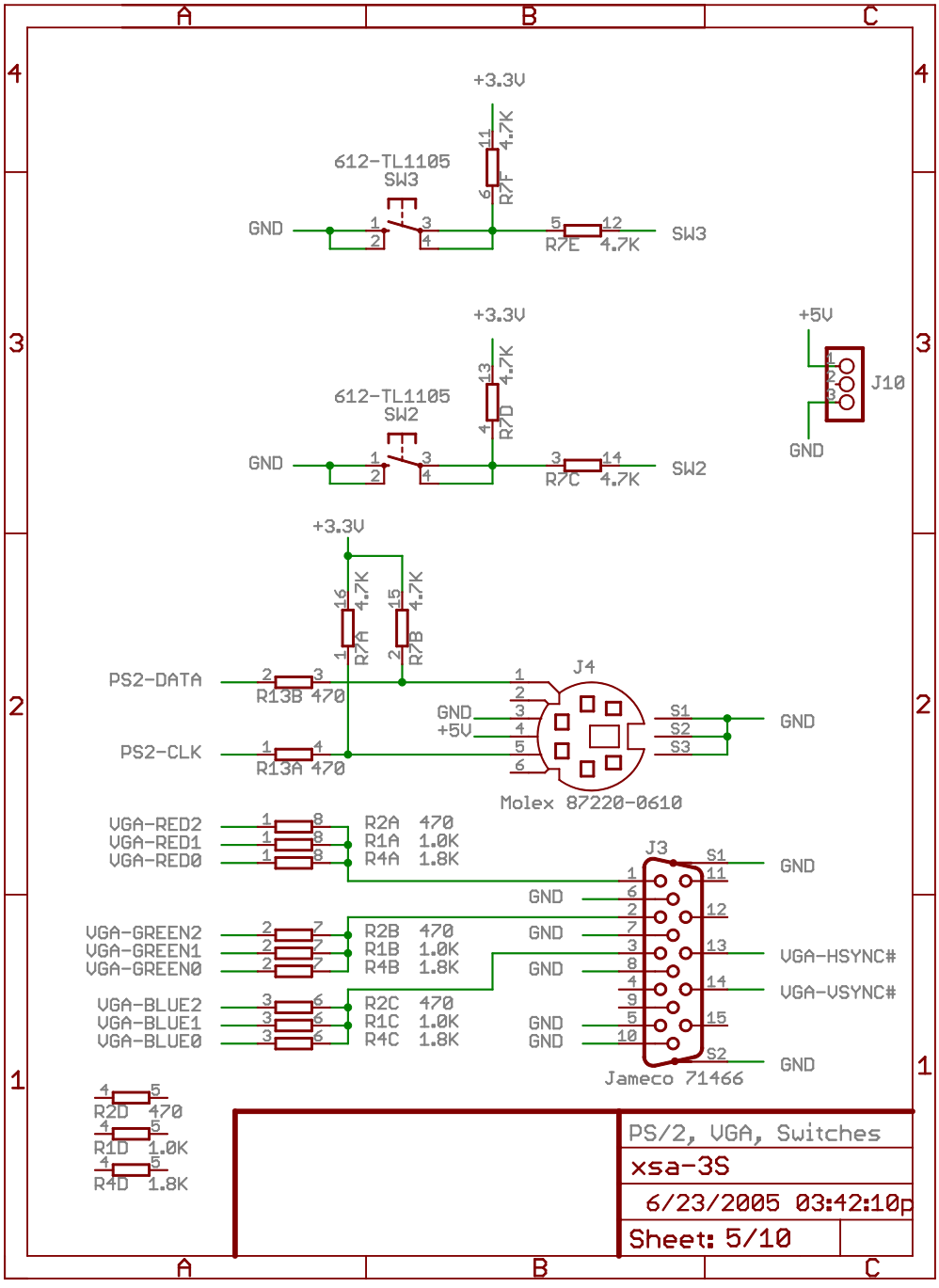
A
B
C
4
3
2
1
+3.3V
612-TL1105
SW3
R7F 4.7K
GND
R7E 4.7K
SW3
+3.3V
612-TL1105
SW2
R7D 4.7K
GND
R7C 4.7K
SW2
+5V
J10
GND
+3.3V
R7A 4.7K
R7B 4.7K
PS2-DATA
R13B 470
PS2-CLK
R13A 470
J4
GND
+5V
S1
S2
S3
GND
Molex 87220-0610
VGA-RED2
VGA-RED1
VGA-RED0
R2A 470
R1A 1.0K
R4A 1.8K
VGA-GREEN2
VGA-GREEN1
VGA-GREEN0
R2B 470
R1B 1.0K
R4B 1.8K
VGA-BLUE2
VGA-BLUE1
VGA-BLUE0
R2C 470
R1C 1.0K
R4C 1.8K
R2D 470
R1D 1.0K
R4D 1.8K
J3
GND
GND
GND
GND
GND
VGA-HSYNC#
VGA-VSYNC#
S1
S2
GND
Jameco 71466
PS/2, VGA, Switches
xsa-3S
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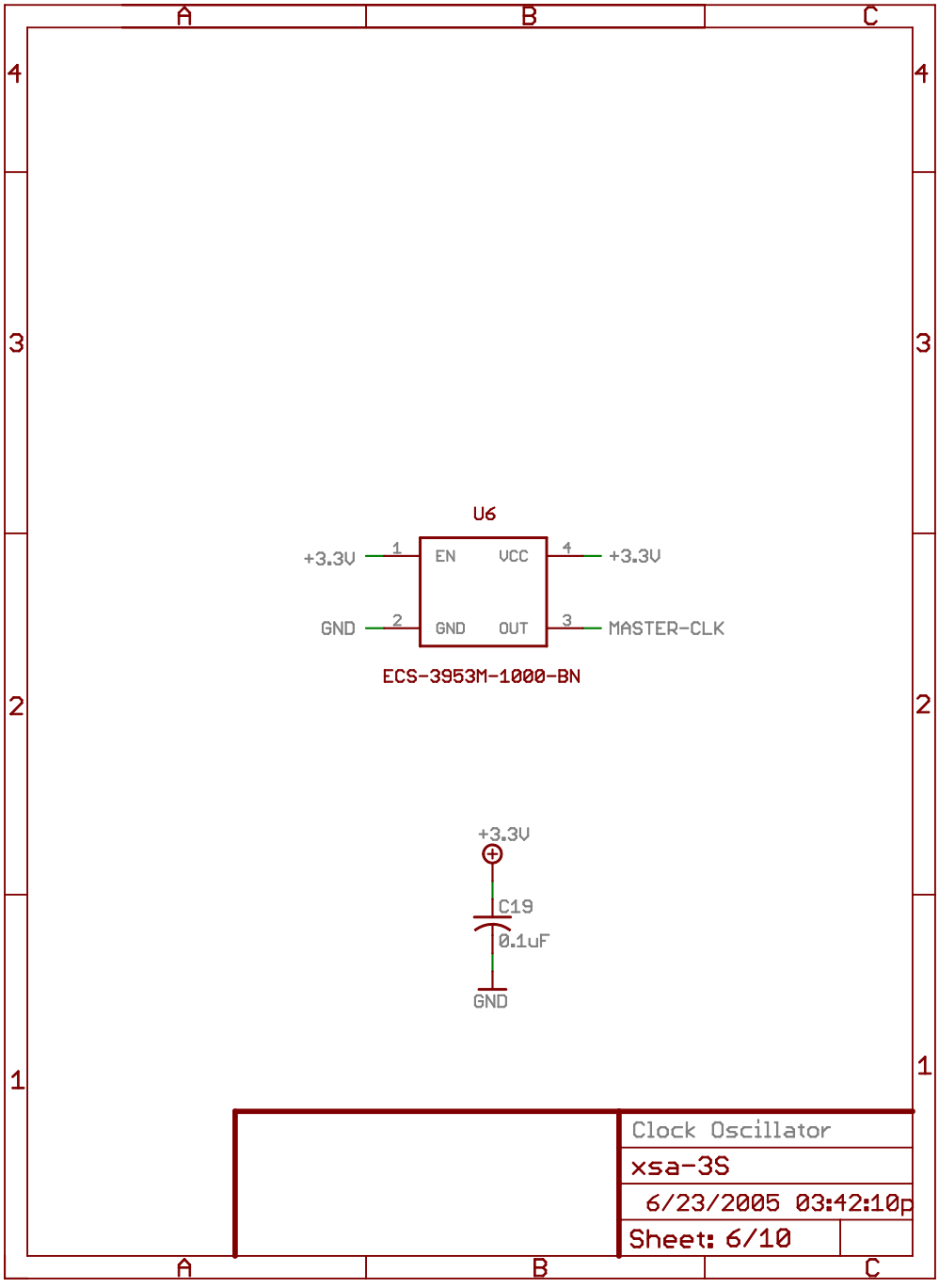
Sheet: 5/10


A
B
C
4
3
2
1
U6
+3.3V
1
EN
VCC
4
+3.3V
GND
2
GND
OUT
3
MASTER-CLK
ECS-3953M-1000-BN
+3.3V
C19
0.1uF
GND
Clock Oscillator
xsa-3S
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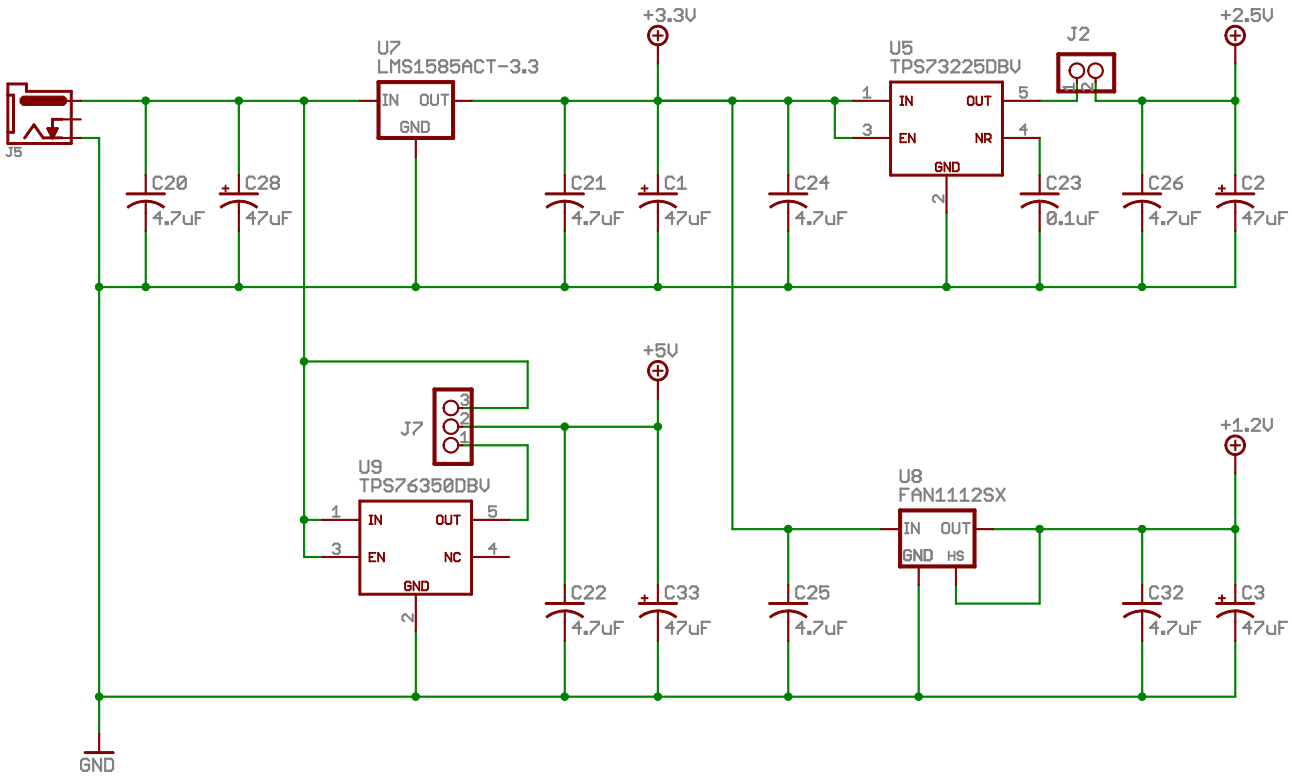
Sheet: 6/10

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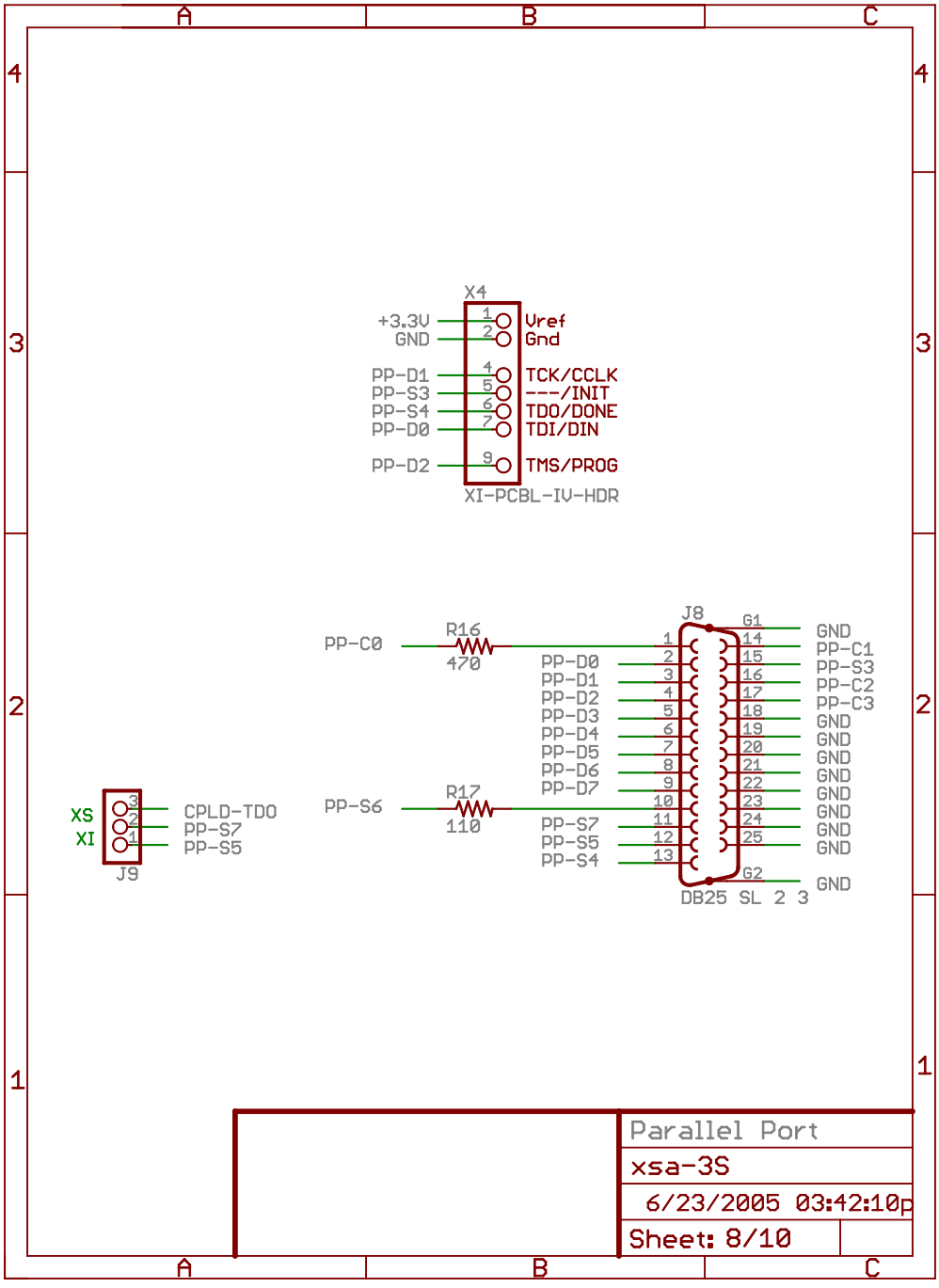
A
B
C
4
3
2
1
X4
+3.3V
GND
PP-D1
PP-S3
PP-S4
PP-D0
PP-D2
1
2
4
5
6
7
9
Vref
Gnd
TCK/CCLK
---/INIT
TDO/DONE
TDI/DIN
TMS/PROG
XI-PCBL-IV-HDR
J8
PP-C0
R16
470
PP-S6
R17
110
PP-D0
PP-D1
PP-D2
PP-D3
PP-D4
PP-D5
PP-D6
PP-D7
PP-S7
PP-S5
PP-S4
G1
G2
GND
PP-C1
PP-S3
PP-C2
PP-C3
DB25 SL 2 3
XS
XI
CPLD-TDO
PP-S7
PP-S5
J9
Parallel Port
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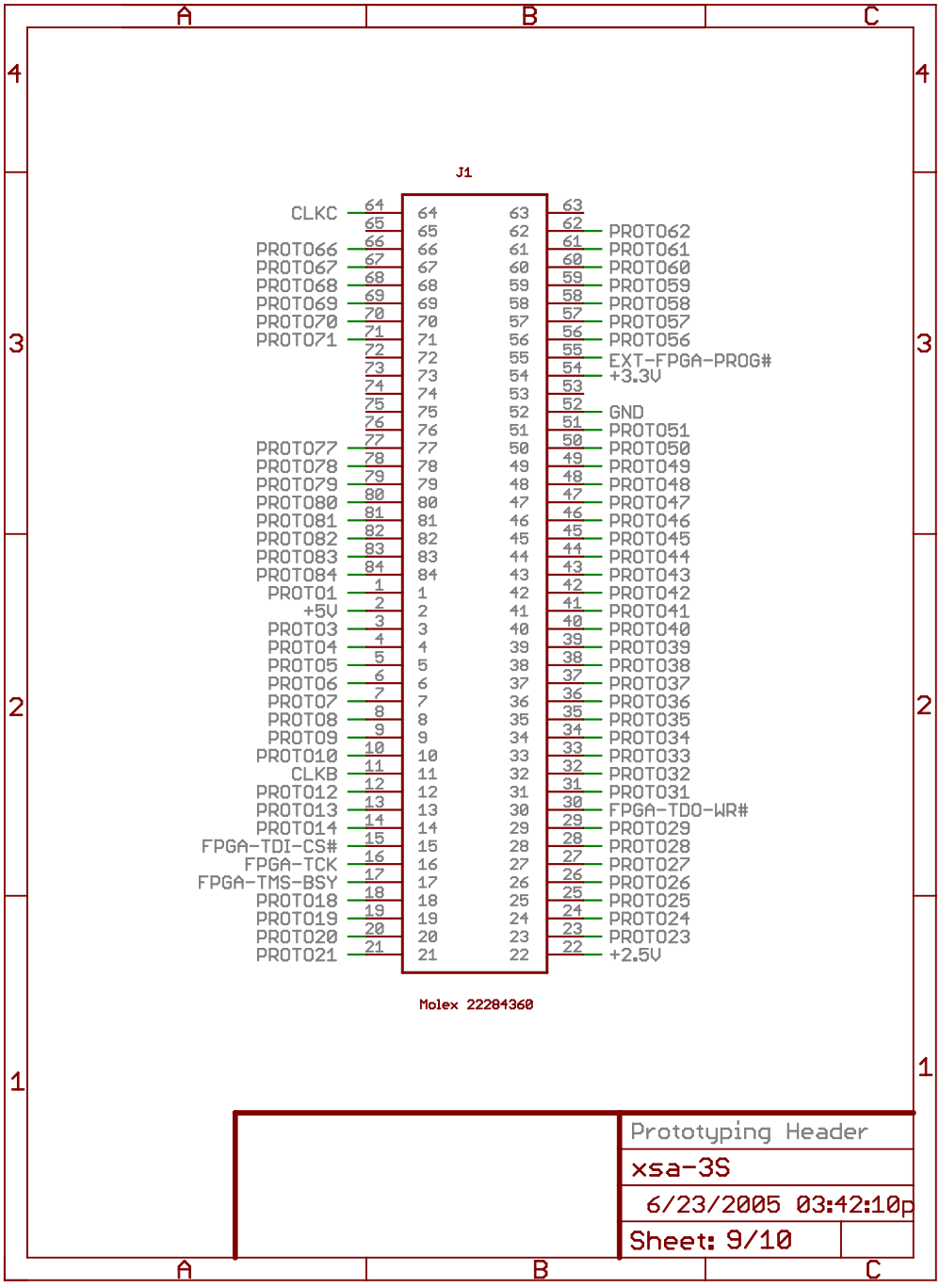
A
B
C
4
3
2
1
J1
CLKC 64
65
PROTO66 66
PROTO67 67
PROTO68 68
PROTO69 69
PROTO70 70
PROTO71 71
72
73
74
75
76
PROTO77 77
PROTO78 78
PROTO79 79
PROTO80 80
PROTO81 81
PROTO82 82
PROTO83 83
PROTO84 84
PROTO1 1
+5V 2
PROTO3 3
PROTO4 4
PROTO5 5
PROTO6 6
PROTO7 7
PROTO8 8
PROTO9 9
PROTO10 10
CLKB 11
PROTO12 12
PROTO13 13
PROTO14 14
FPGA-TDI-CS# 15
FPGA-TCK 16
FPGA-TMS-BSY 17
PROTO18 18
PROTO19 19
PROTO20 20
PROTO21 21
64 63
65 62
66 61
67 60
68 59
69 58
70 57
71 56
72 55
73 54
74 53
75 52
76 51
77 50
78 49
79 48
80 47
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82 45
83 44
84 43
1 42
2 41
3 40
4 39
5 38
6 37
7 36
8 35
9 34
10 33
11 32
12 31
13 30
14 29
15 28
16 27
17 26
18 25
19 24
20 23
21 22
63
62 PROTO62
61 PROTO61
60 PROTO60
59 PROTO59
58 PROTO58
57 PROTO57
56 PROTO56
55 EXT-FPGA-PROG#
54 +3.3V
53
52 GND
51 PROTO51
50 PROTO50
49 PROTO49
48 PROTO48
47 PROTO47
46 PROTO46
45 PROTO45
44 PROTO44
43 PROTO43
42 PROTO42
41 PROTO41
40 PROTO40
39 PROTO39
38 PROTO38
37 PROTO37
36 PROTO36
35 PROTO35
34 PROTO34
33 PROTO33
32 PROTO32
31 PROTO31
30 FPGA-TDO-WR#
29 PROTO29
28 PROTO28
27 PROTO27
26 PROTO26
25 PROTO25
24 PROTO24
23 PROTO23
22 +2.5V
Molex 22284360
Prototyping Header
xsa-3S
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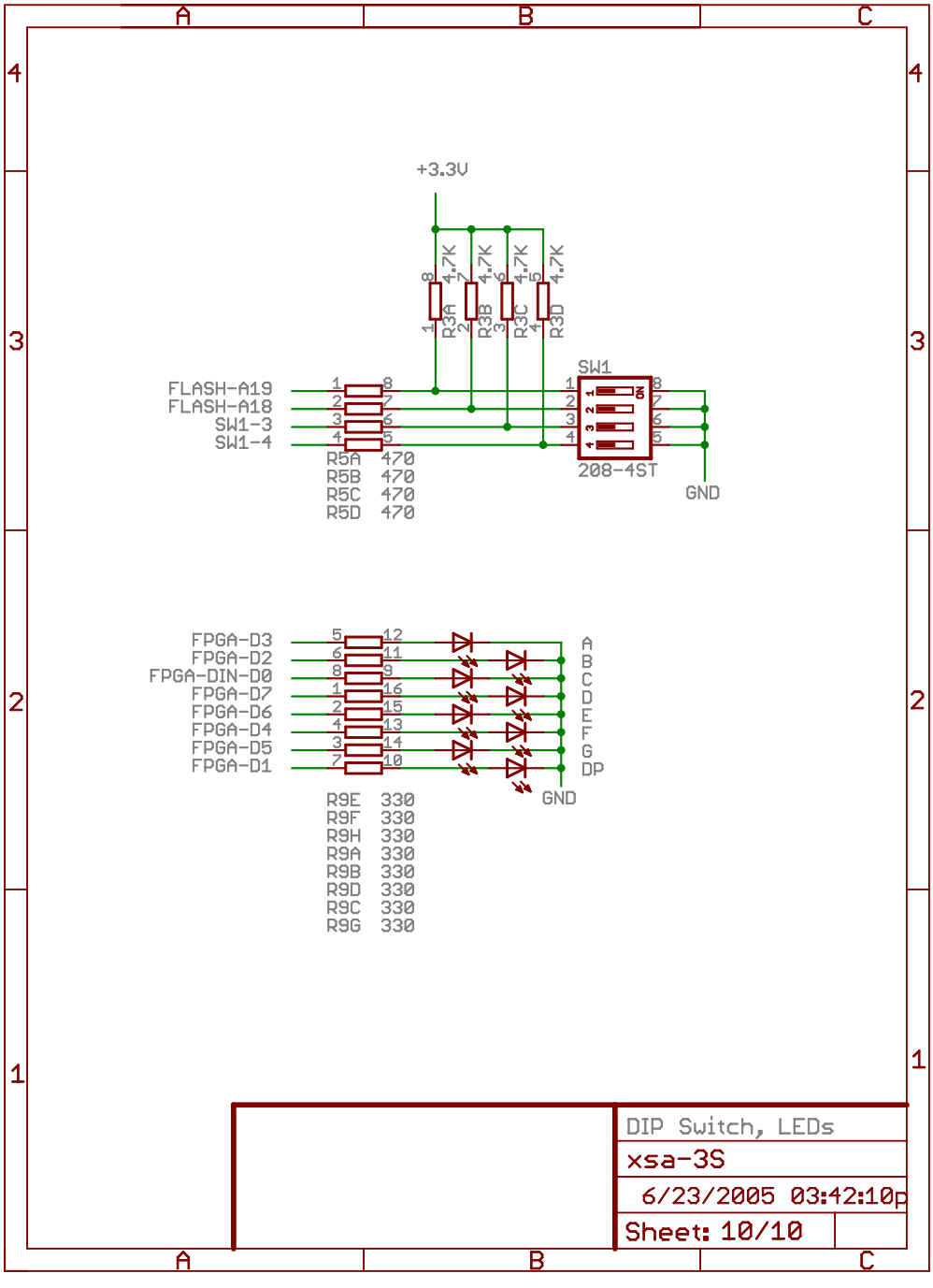
A
B
C
4
3
2
1
+3.3V
R3A 4.7K
R3B 4.7K
R3C 4.7K
R3D 4.7K
SW1
208-4ST
FLASH-A19
FLASH-A18
SW1-3
SW1-4
R5A 470
R5B 470
R5C 470
R5D 470
GND
FPGA-D3
FPGA-D2
FPGA-DIN-D0
FPGA-D7
FPGA-D6
FPGA-D4
FPGA-D5
FPGA-D1
A
B
C
D
E
F
G
DP
GND
R9E 330
R9F 330
R9H 330
R9A 330
R9B 330
R9D 330
R9C 330
R9G 330
DIP Switch, LEDs
xsa-3S
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